TS12A12511 具有负信号处理功能的 5Ω 单通道 SPDT 模拟开关

1 特性

- ±2.7V 至 ±6V 双电源
- 2.7V 至 12V 单电源
- 5Ω（典型值）导通状态电阻
- 1.6Ω（典型值）导通状态电阻平坦度
- 3.3V、5V 兼容数字控制输入
- 轨到轨模拟信号处理
- 快速 t_{ON}、t_{OFF} 时间
- 支持数字和模拟信号应用
- 微型 8 引线 SOT-23、8 引线 MSOP 和 QFN-8 封装
- 闩锁性能超过 100 mA，符合 JESD 78 II 类规范
- ESD 性能经测试符合 JESD 22 规范
  - ±2000V 人体放电模型（A114-B，II 类）
  - ±1000V 组件充电模式 (C101)

2 应用

- 自动测试设备
- 电源布线
- 通信系统
- 数据采集系统
- 采样保持系统
- 继电器更换
- 电网基础设施

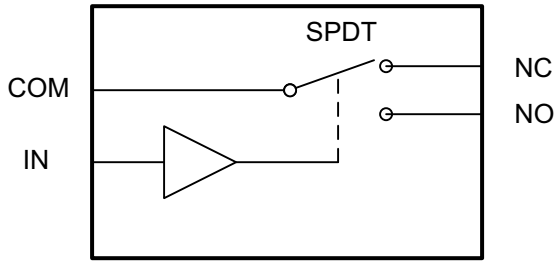
3 说明

TS12A12511 是一款双向单通道单极双投 (SPDT) 模拟开关，可传递摆幅为 0V 至 12V 或 -6V 至 6V 的信号。此开关开启时，在两个方向上都表现得很好。该器件还具备 5Ω（典型值）的低导通状态电阻，与通道间电阻的差额小于 1Ω。其最大电流消耗小于 1μA，-3dB 带宽大于 93MHz。TS12A12511 具有先断后合开关操作，可防止切换通道时发生瞬时短路。此器件可采用 8 引线 VSSOP、8 引线 SOT-23 和 8 引脚 WSON 封装。

封装信息(1)

器件型号	封装	封装尺寸（标称值）
TS12A12511	DCN（SOT-23，8）	2.90mm × 1.63mm
	DGK（VSSOP，8）	3.00mm × 3.00mm
	DRJ（WSON，8）	4.00mm × 4.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



简化原理图

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision D (January 2019) to Revision E (September 2022) — **Page**

- 更新了整个文档中的表格、图和交叉参考的编号格式 1
- 更新了*应用*部分 1
- Updated the *Leakage Current vs I/O Voltage (Switch ON)* and *Leakage Current vs I/O Voltage (Switch OFF)* figures 8

Changes from Revision C (January 2015) to Revision D (January 2019) — **Page**

- Added Junction temperature to the *Absolute Maximum Ratings* table 4

Changes from Revision B (April 2011) to Revision C (January 2015) — **Page**

- 添加了*引脚配置和功能*部分、*ESD 等级*表、*特性说明*部分、*器件功能模式*、*应用和实施*部分、*电源相关建议*部分、*布局*部分、*器件和文档支持*部分以及*机械、封装和可订购信息*部分 1

Changes from Revision A (May 2010) to Revision B (April 2011) — **Page**

- Deleted preview status from DGK and DCN packages 3

5 Pin Configuration and Functions

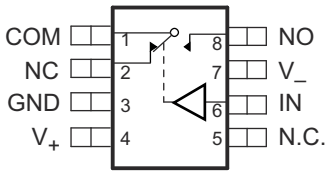


图 5-1. DGK Package, 8-Pin VSSOP (Top View)

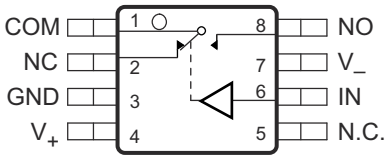
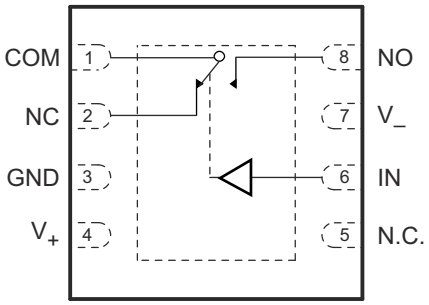


图 5-2. DCN Package, 8-Pin SOT-23 (Top View)



N.C. – Not internally connected NC – Normally closed NO – Normally open
The Exposed Thermal Pad must be electrically connected to V– or left floating.

图 5-3. DRJ Package, 8-Pin WSON (Top View)

表 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
COM	1	I/O	Common. Can be an input or output.
GND	3	—	Ground (0 V) reference
IN	6	I	Logic control input
NC	2	I/O	Normally closed. Can be an input or output.
N.C.	5	—	No connect. Not internally connected.
NO	8	I/O	Normally open. Can be an input or output.
V_{CC}	4	I	Most positive power supply
$-V_{CC}$	7	I	Most negative power supply. This pin is only used in dual-supply applications and should be tied to ground in single-supply applications.
Thermal pad		—	The Exposed Thermal Pad must be electrically connected to V– or left floating.

(1) I = input, O = output

6 Specifications

6.1 Absolute Maximum Ratings

T_A = 25°C (unless otherwise noted).(1)

			MIN	MAX	UNIT
V_{CC} to $-V_{CC}$			0	13	V
V_{CC} to GND			–0.3	13	V
$-V_{CC}$ to GND			–6.5	0.3	V
$V_{I/O}$	Analog inputs	NC, NO, or COM	$-V_{CC}$ – 0.5	V_{CC} + 0.5	V
I_{IN}	Digital inputs			±30	mA
$I_{I/O}$	Peak current	NC, NO, or COM		±100	mA
	Continuous current	NC, NO, or COM		±50	mA
T_A	Operating temperature		–40	85	°C
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under 节 6.3 is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
V_{CC}	0	12	V
$-V_{CC}$	–6	0	V
$V_{I/O}$	$-V_{CC}$	V_{CC}	V
V_{IN}	0	V_{CC}	V

6.4 Thermal Information

THERMAL METRIC(1)		TS12A12511			UNIT
		DCN	DGK	DRJ	
		8 PINS			
$R_{\theta JA}$	Junction-to-ambient thermal resistance	218.4	184.5	47.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	89.9	71.0	48.6	
$R_{\theta JB}$	Junction-to-board thermal resistance	144.4	104.5	24.2	
ψ_{JT}	Junction-to-top characterization parameter	7.8	11.3	1.2	
ψ_{JB}	Junction-to-board characterization parameter	141.7	103.3	24.4	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	9.0	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics: ±5-V Dual Supply

V_{CC} = 5 V ± 10%, $-V_{CC}$ = – 5 V ± 10%, T_A = – 40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A= 25°C			T_A= – 40°C to 85°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
ANALOG SWITCH									
	Analog signal range					$-V_{CC}$		V_{CC}	V
R_{ON}	ON-state resistance	V_{NC} = -4.5 V to +4.5 V or V_{NO} = – 4.5 V to 4.5 V, I_{COM} = – 10 mA; see 图 7-1		5			5	8	Ω
ΔR_{ON}	ON-state resistance match between channels	V_{NC} = -4.5 V to +4.5 V or V_{NO} = -4.5 V to +4.5 V, I_{COM} = – 10 mA		1	1.2			1.6	Ω
$R_{ON(flat)}$	ON-state resistance flatness	V_{NC} = -3.3 V to +3.3 V or V_{NO} = -3.3 V to +3.3 V, I_{COM} = – 10 mA		1.6	2.2			2.2	Ω
LEAKAGE CURRENTS									
$I_{NC(OFF)}$, $I_{NO(OFF)}$	OFF leakage current	V_{NC} = -4.5 V to +4.5 V or V_{NO} = -4.5 V to +4.5 V V_{COM} = -4.5 V to +4.5 V; see 图 7-2	– 1	±0.5	1	– 50		50	nA
$I_{NC(ON)}$, $I_{NO(ON)}$	ON leakage current	V_{NC} = -4.5 V to +4.5 V or V_{NO} = -4.5 V to +4.5 V V_{COM} = open; see 图 7-3	– 1	±0.5	1	– 50		50	nA
DIGITAL INPUTS									
V_{INH}	High-level input voltage					2.4		V_{CC}	V
V_{INL}	Low-level input voltage					0		0.8	V
I_{INL}, I_{INH}	Input current	V_{IN} = V_{INL} or V_{INH}		0.005		– 1		1	μA
C_{IN}	Control input capacitance			2.5					pF
DYNAMIC(1)									
t_{ON}	Turn-ON time	R_L = 300 Ω, C_L = 35 pF, V_{COM} = 3.3 V; see 图 7-5		80	95			115	ns
t_{OFF}	Turn-OFF time	R_L = 300 Ω, C_L = 35 pF, V_{COM} = 3.3 V		41	50			56	ns
t_{BBM}	Break-before-make time delay	R_L = 300 Ω, C_L = 35 pF, V_{NC} = V_{NO} = 3.3 V; see 图 7-6		36		18			ns
Q_C	Charge injection	V_{NC} = V_{NO} = 0 V, R_{GEN} = 0 Ω, C_L = 1 nF; see 图 7-7		26					pC
O_{ISO}	OFF isolation	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see 图 7-8		– 70					dB
X_{TALK}	Channel-to-channel crosstalk	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see 图 7-9		– 70					dB
BW	Bandwidth – 3 dB	R_L = 50 Ω, C_L = 5 pF; see 图 7-10		93					MHz
THD	Total harmonic distortion	R_L = 600 Ω, C_L = 15pF, VNO = $1V_{RMS}$, f = 20 kHz; see 图 7-11		0.004%					
$C_{NC(OFF)}$, $C_{NO(OFF)}$	NC, NO OFF capacitance	f = 1 MHz; see 图 7-4		14					pF
$C_{COM(ON)}$, $C_{NC(ON)}$, $C_{NO(ON)}$	COM, NC, NO ON capacitance	f = 1 MHz; see 图 7-4		60					pF
SUPPLY									
I_{CC}	Positive supply current			0.03				1	μA

(1) Specified by design, not subject to production test.

6.6 Electrical Characteristics: 12-V Single Supply

V_{CC} = 12 V ± 10%, -V_{CC} = 0 V, GND = 0 V, T_A = – 40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A= 25°C			T_A= – 40°C to 85°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
ANALOG SWITCH									
	Analog signal range					0		V_{CC}	V
R_{on}	ON-state resistance	V_{NC} =0 V to 10.8 V or V_{NO} = 0 V to 10.8 V, I_{COM} = – 10 mA, see 图 7-1		5			5	8	Ω
ΔR_{on}	ON-state resistance match between channels	V_{NC} = 0 V to 10.8 V or V_{NO} = 0 V to 10.8 V, I_{COM} = – 10 mA		1.6	2.4			2.6	Ω
$R_{on(flat)}$	ON-state resistance flatness	V_{NC} = 3.3 V to 7V or V_{NO} = 3.3 V to 7 V, I_{COM} = – 10 mA		1.7			1.8	3.2	Ω
LEAKAGE CURRENTS									
$I_{NC(OFF)}$, $I_{NO(OFF)}$	OFF leakage current	V_{NC} = 0 V to 10.8 V or V_{NO} = 0 V to 10.8 V, V_{COM} = 0 V to 10.8 V; see 图 7-2	– 10	±0.5	10	– 50		50	nA
$I_{NC(ON)}$, $I_{NO(ON)}$	ON leakage current	V_{NC} = 0 V to 10.8V or V_{NO} = 0 V to 10.8 V, V_{COM} = open; see 图 7-3	– 10	±0.5	10	– 50		50	nA
DIGITAL INPUTS									
V_{INH}	High-level input voltage					5		V_{CC}	V
V_{INL}	Low-level input voltage					0		0.8	V
I_{INL}, I_{INH}	Input current	V_{IN} = V_{INL} or V_{INH}		±0.005		– 0.1		0.1	μA
C_{IN}	Digital input capacitance			2.7					pF
DYNAMIC (1)									
t_{ON}	Turn-ON time	R_L = 300 Ω, C_L = 35 pF, V_{COM} = 3.3 V; see 图 7-5		56	85			110	ns
t_{OFF}	Turn-OFF time	R_L = 300 Ω, C_L = 35 pF, V_{COM} = 3.3 V; see 图 7-5		25	30			31	ns
t_{BBM}	Break-before-make time delay	R_L = 300 Ω, C_L = 35 pF, V_{NC} = V_{NO} = 3.3 V; see 图 7-6		30		19			ns
Q_C	Charge injection	R_{GEN} = V_{NC} = V_{NO} = 0 V, R_{GEN} = 0 Ω, C_L = 1 nF; see 图 7-7		491					pC
O_{ISO}	OFF isolation	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see 图 7-8		– 70					dB
X_{TALK}	Channel-to-channel crosstalk	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see 图 7-9		– 70					dB
BW	Bandwidth – 3 dB	R_L = 50 Ω, C_L = 5 pF, see 图 7-10		200					MHz
THD	Total harmonic distortion	R_L = 600 Ω, C_L = 15pF, V_{NO} = 1 V_{RMS}, f = 20 kHz; see 图 7-11		0.04%					
$C_{NC(OFF)}$, $CI_{NO(OFF)}$	NC, NO OFF capacitance	f = 1 MHz, see 图 7-4		14					pF
$C_{COM(ON)}$, $C_{NC(ON)}$, $C_{NO(ON)}$	COM, NC, NO ON capacitance	f = 1 MHz, see 图 7-4		55					pF
SUPPLY									
I_{CC}	Positive supply current			0.07				1	μA

(1) Specified by design, not subject to production test.

6.7 Electrical Characteristics: 5-V Single Supply

V_{CC} = 5 V ± 10%, -V_{CC} = 0 V, GND = 0 V, T_A = – 40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A= 25°C			T_A= – 40°C to 85°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
ANALOG SWITCH									
	Analog signal range					0		V_{CC}	V
R_{on}	ON-state resistance	V_{NC} =0 V to 4.5 V or V_{NO} = 0 V to 4.5 V, I_{COM} = – 10 mA; see 图 7-1		8	10			12.5	Ω
ΔR_{on}	ON-state resistance match between channels	V_{NC} =0 V to 4.5 V or V_{NO} = 0 V to 4.5 V, I_{COM} = – 10 mA		1	1.1			1.5	Ω
$R_{on(flat)}$	ON-state resistance flatness	V_{NC} =0 V to 4.5 V or V_{NO} = 0 V to 4.5 V, I_{COM} = – 10 mA		1.3			1.3	2	Ω
LEAKAGE CURRENTS									
$I_{NC(OFF)}$, $I_{NO(OFF)}$	OFF leakage current	V_{NC} =0 V to 4.5 V or V_{NO} = 0 V to 4.5 V, V_{COM} = 0 V to 4.5 V; see 图 7-2	– 1	±0.5	1	– 50		50	nA
$I_{NC(ON)}$, $I_{NO(ON)}$	ON leakage current	V_{NC} = 0 V to 4.5V or V_{NO} = 0 V to 4.5 V, V_{COM} = open; see 图 7-3	– 1	±0.5	1	– 50		50	nA
DIGITAL INPUTS									
V_{INH}	High-level input voltage					2.4		V_{CC}	V
V_{INL}	Low-level input voltage					0		0.8	V
I_{INL}, I_{INH}	Input current	V_{IN} = V_{INL} or V_{INH}		0.01		– 0.1		0.1	μA
C_{IN}	Digital input capacitance			2.8					pF
DYNAMIC(1)									
t_{ON}	Turn-ON time	R_L = 300 Ω, C_L = 35 pF, V_{COM} = 3.3 V; see 图 7-5		119	145			178	ns
t_{OFF}	Turn-OFF time	R_L = 300 Ω, C_L = 35 pF, V_{COM} = 3.3 V; see 图 7-5		38	47			95.2	ns
t_{BBM}	Break-before-make time delay	R_L = 300 Ω, C_L = 35 pF, V_{NC} = V_{NO} = 3.3 V; see 图 7-6		79		44			ns
Q_C	Charge injection	V_{GEN} = V_{NC} = V_{NO} = 0 V, R_{GEN} = 0 Ω, C_L = 1 nF; see 图 7-7		65					pC
O_{ISO}	OFF isolation	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see 图 7-8		– 70					dB
X_{TALK}	Channel-to-channel crosstalk	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see 图 7-9		– 70					dB
BW	Bandwidth – 3 dB	R_L = 50 Ω, see 图 7-10		152					MHz
THD	Total harmonic distortion	R_L = 600 Ω, C_L = 15 pF, V_{NO} = 1 VRMS, f = 20 kHz; see 图 7-11		0.04%					
$C_{NC(OFF)}$, $C_{NO(OFF)}$	NC, NO OFF capacitance	f = 1 MHz, see 图 7-4		15					pF
$C_{COM(ON)}$, $C_{NC(ON)}$, $I_{NO(ON)}$	COM, NC, NO ON capacitance	f = 1 MHz, see 图 7-4		55					pF
POWER REQUIREMENTS									
I_{CC}	Positive supply current	V_{IN} = 0 V or V_{CC}		0.02				1	μA

(1) Specified by design, not subject to production test.

6.8 Typical Characteristics

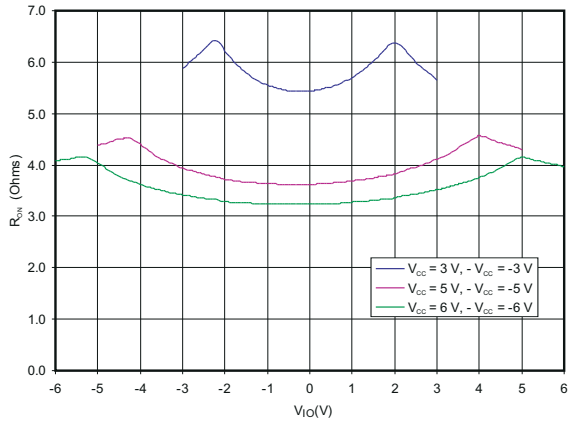


图 6-1. R_{ON} vs V_{IO}

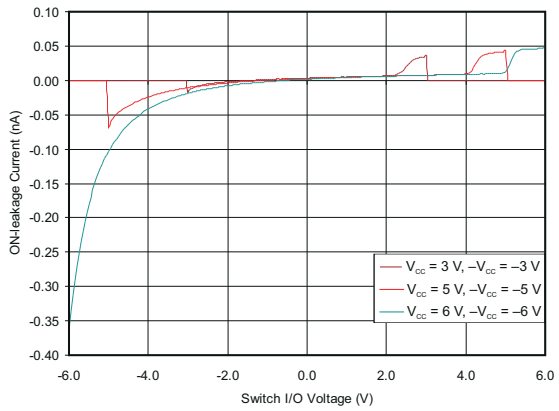


图 6-2. Leakage Current vs I/O Voltage (Switch ON)

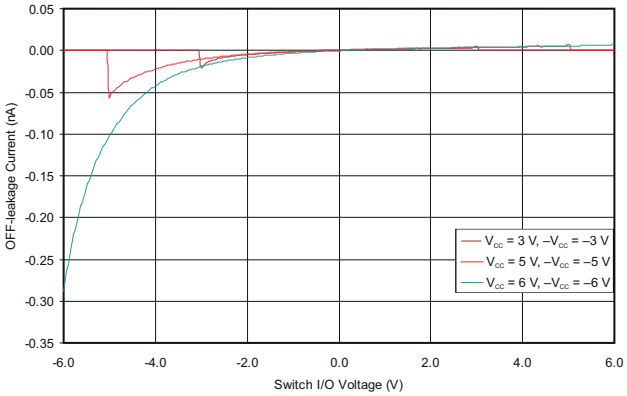


图 6-3. Leakage Current vs I/O Voltage (Switch OFF)

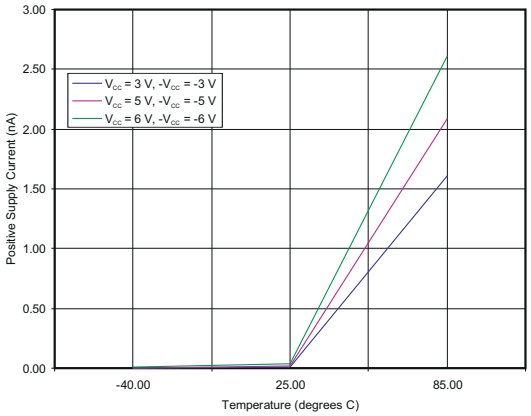


图 6-4. Positive Supply Current vs Temperature

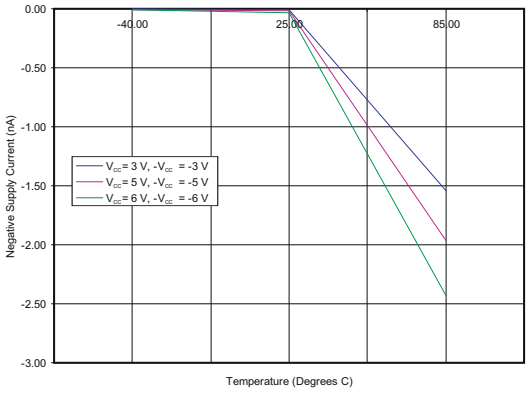


图 6-5. Negative Supply Current vs Temperature

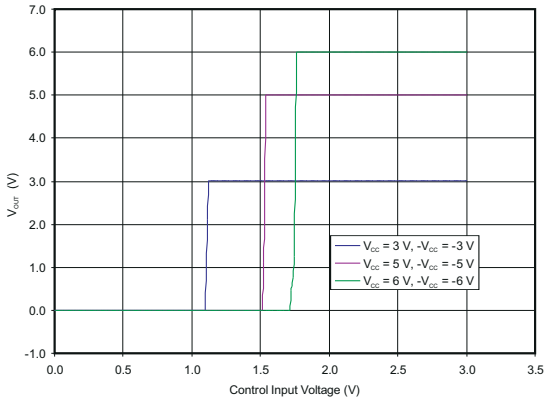


图 6-6. Control Input (IN) Threshold Voltage

6.8 Typical Characteristics (continued)

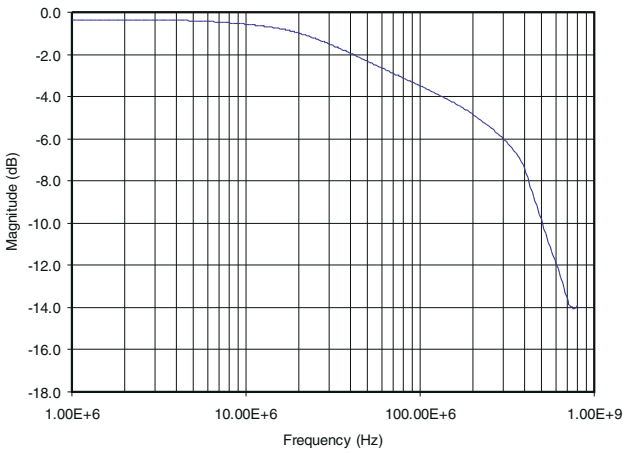


图 6-7. Bandwidth Dual Supply (±5 V)

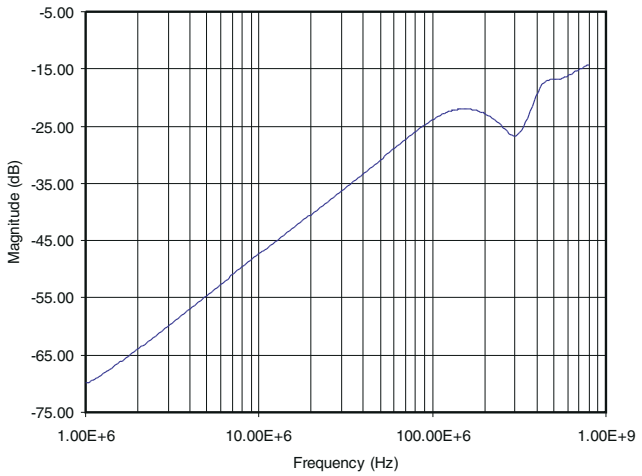


图 6-8. Off Isolation vs Frequency Dual Supply (±5 V)

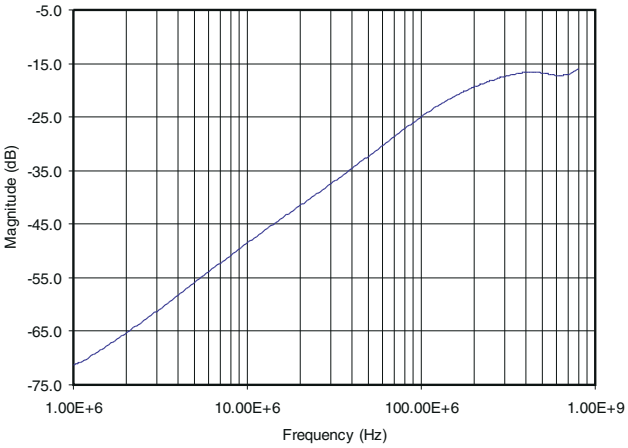


图 6-9. Crosstalk vs Frequency Dual Supply (±5 V)

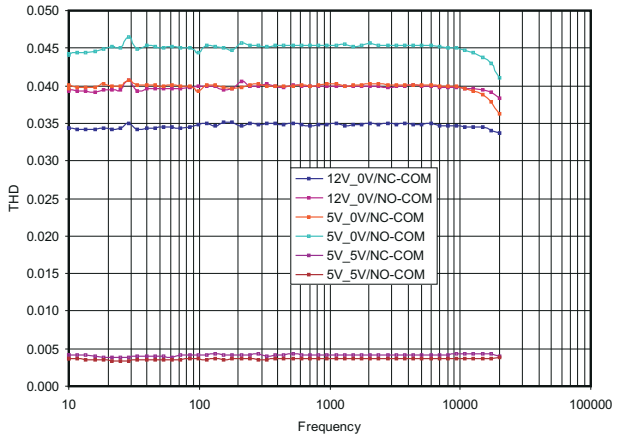


图 6-10. THD+N (%) vs Frequency

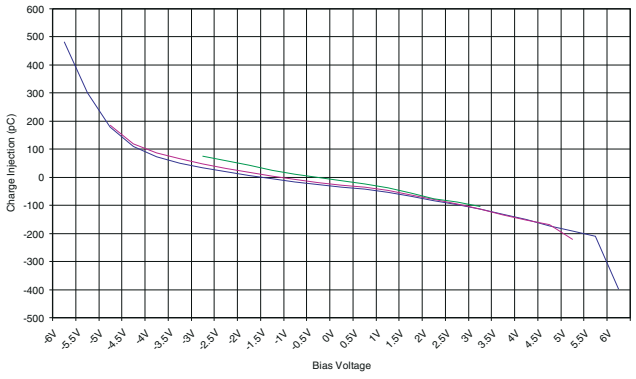
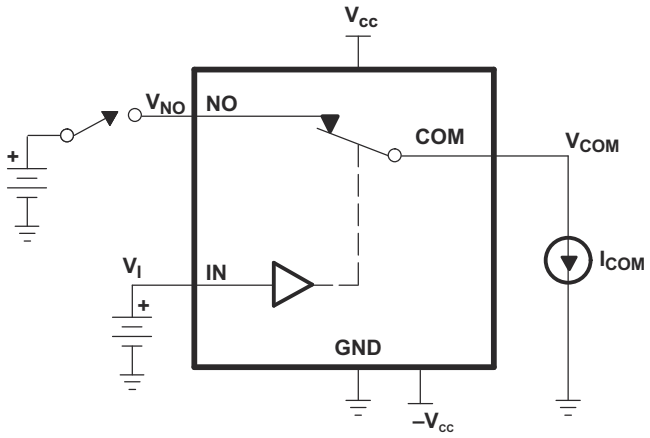


图 6-11. Charge Injection vs Bias Voltage

7 Parameter Measurement Information

7.1 Test Circuits

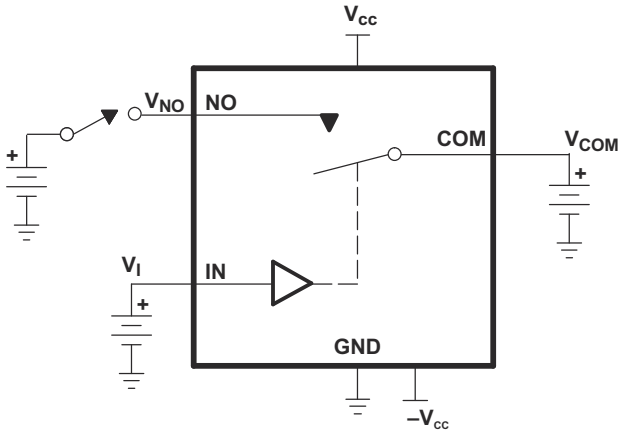


Channel ON

$R_{on} = \frac{V_{COM} - V_{NO}}{I_{COM}}$

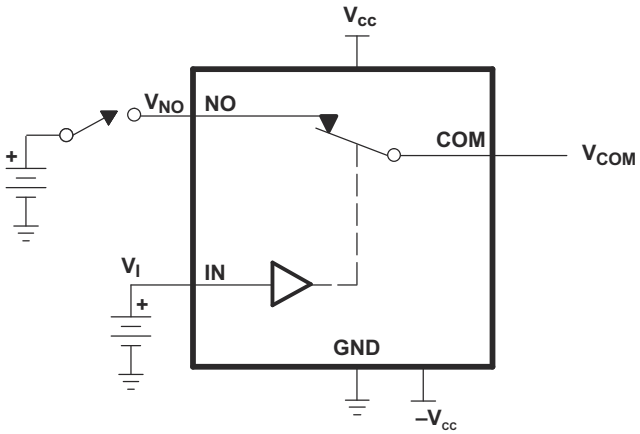
$V_I = V_{IH}$ or V_{IL}

图 7-1. ON-State Resistance



OFF-State Leakage Current
Channel OFF
$V_I = V_{IH}$ or V_{IL}

图 7-2. OFF-State Leakage Current ($I_{COM(OFF)}$, $I_{NC(OFF)}$)



ON-State Leakage Current
Channel ON
$V_I = V_{IH}$ or V_{IL}

图 7-3. ON-State Leakage Current ($I_{COM(ON)}$, $I_{NC(ON)}$)

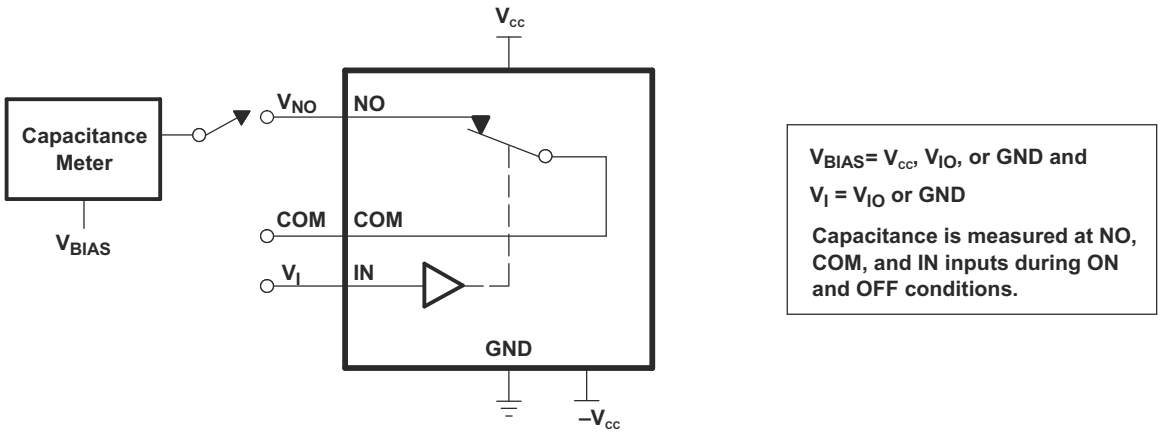
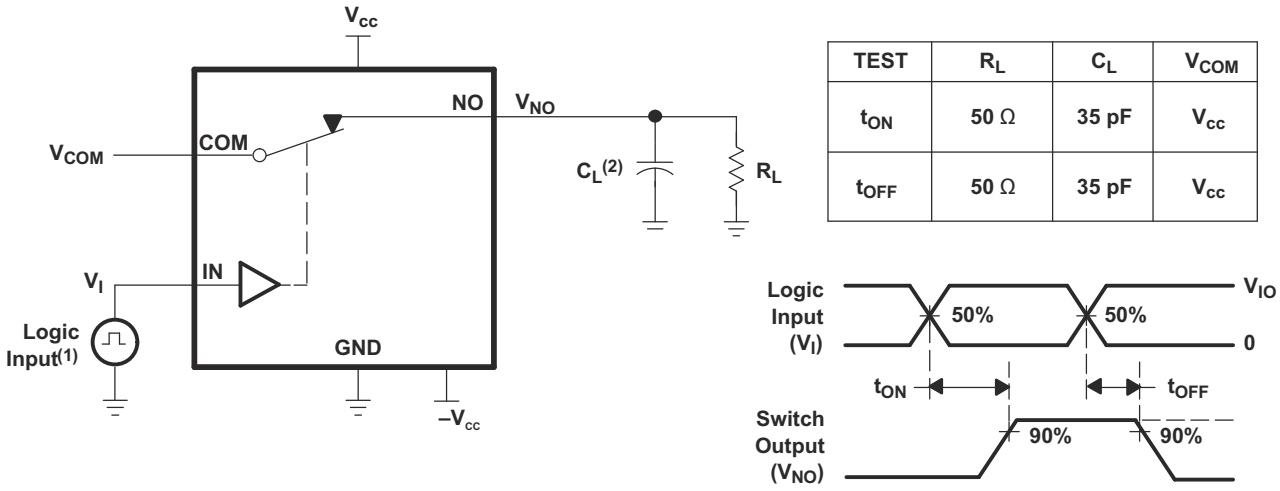
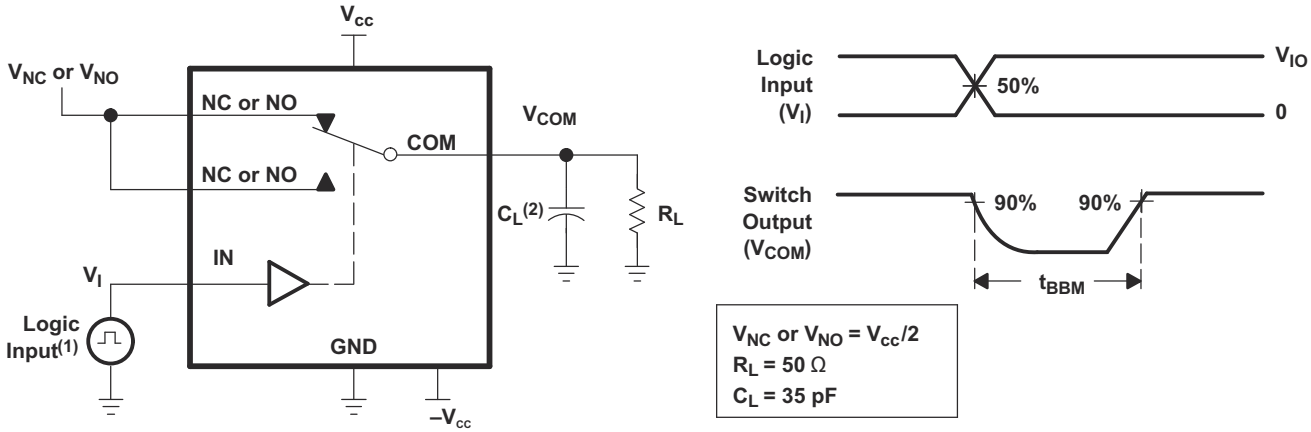


图 7-4. Capacitance ($C_{COM(OFF)}$, $C_{COM(ON)}$, $C_{NC(OFF)}$, $C_{NC(ON)}$)



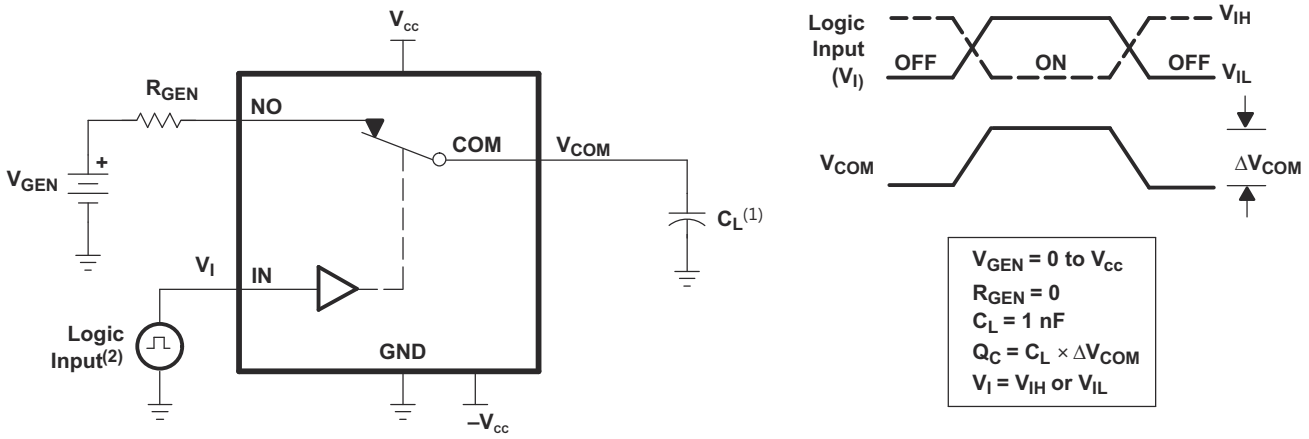
(1) All input pulses are supplied by generators having the following characteristics: PRR≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.
(2) C_L includes probe and jig capacitance.

图 7-5. Turn-ON (t_{ON}) and Turn-OFF Time (t_{OFF})



(1) All input pulses are supplied by generators having the following characteristics: PRR≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.
(2) C_L includes probe and jig capacitance.

图 7-6. Break-Before-Make Time Delay (t_{BBM})



(1) C_L includes probe and jig capacitance.
(2) All input pulses are supplied by generators having the following characteristics: PRR≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

图 7-7. Charge Injection (Q_C)

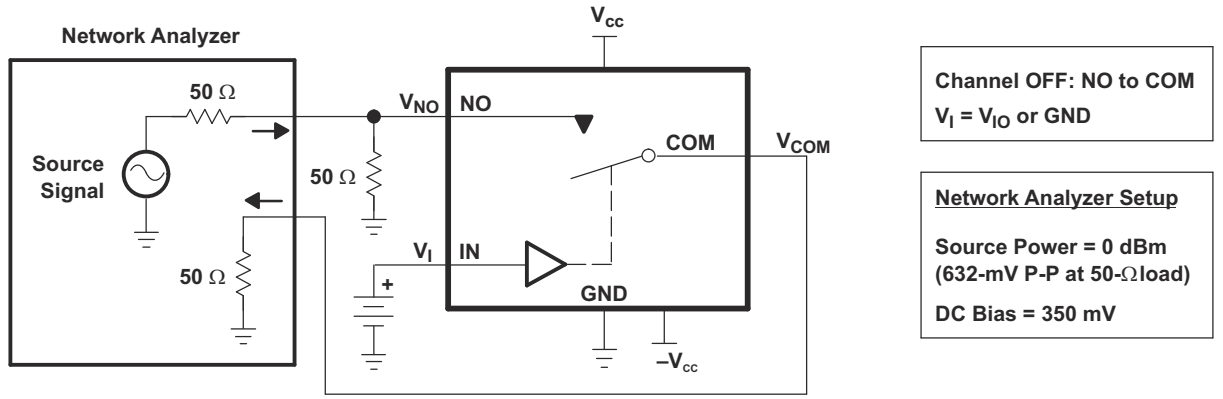


图 7-8. OFF Isolation (O_{ISO})

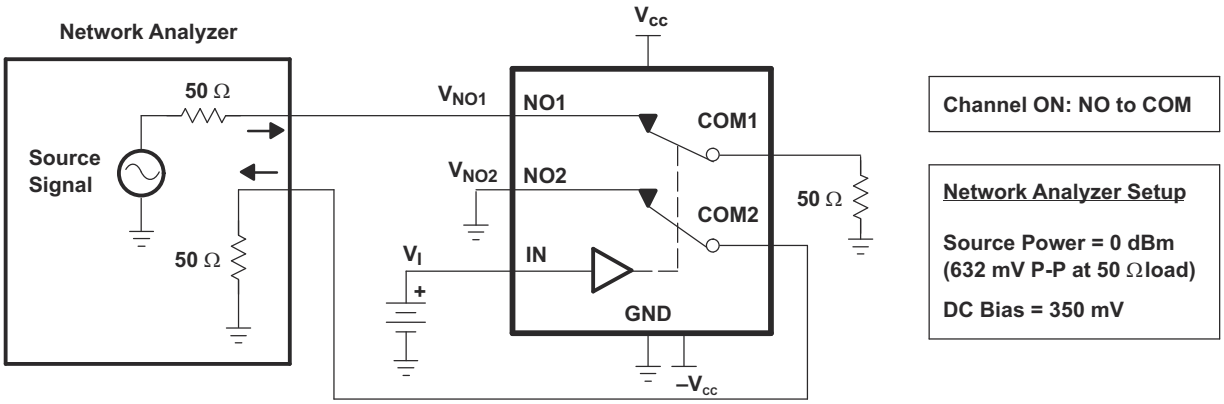


图 7-9. Channel-to-Channel Crosstalk (X_{TALK})

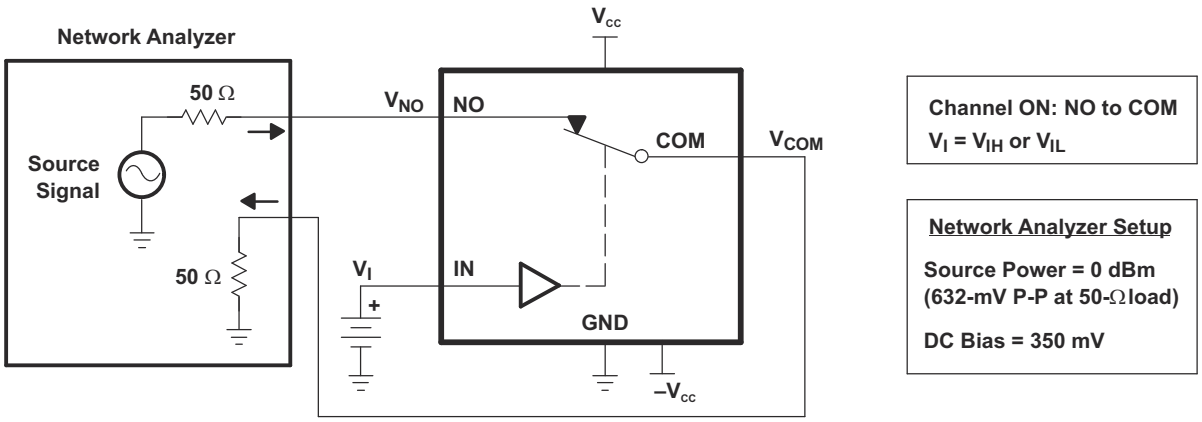
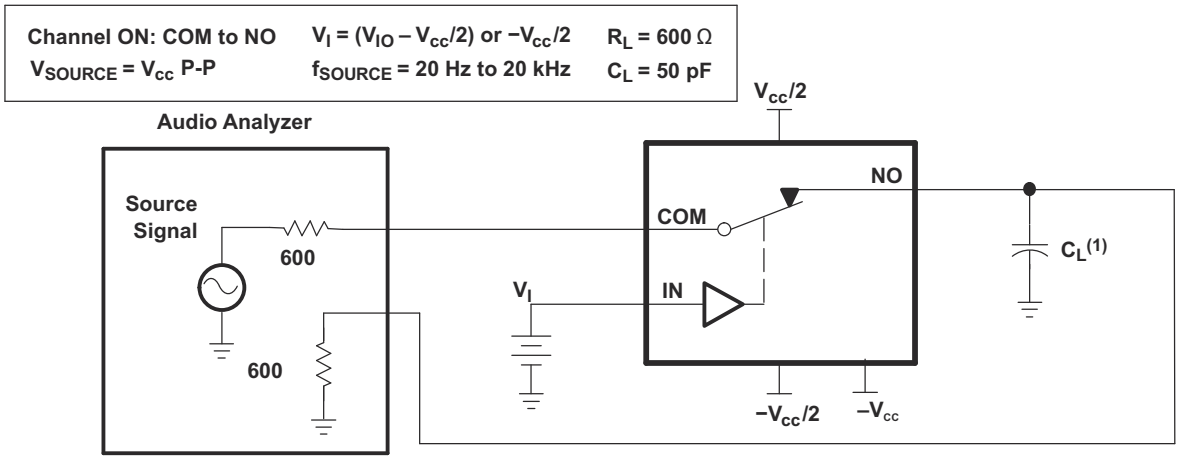


图 7-10. Bandwidth (BW)



(1) C_L includes probe and jig capacitance.

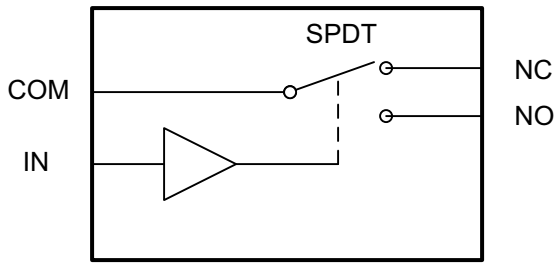
图 7-11. Total Harmonic Distortion

8 Detailed Description

8.1 Overview

The TS12A12511 is a bidirectional, single channel, single-pole double-throw (SPDT) analog switch that can pass signals with swings of 0 to 12 V or – 6 V to 6 V. This switch conducts equally well in both directions when it is on. It also offers a low ON-state resistance of 5 Ω (typical), which is matched to within 1 Ω between channels. The maximum current consumption is < 1 μA and – 3 dB bandwidth is > 93 MHz. The TS12A12511 exhibits break-before-make switching action, preventing momentary shorting when switching channels. This device is available in an 8-lead MSOP, 8-lead SOT-23, and 8-pin QFN package.

8.2 Functional Block Diagram



8.3 Feature Description

The TS12A12511 can pass signals with swings of 0 to 12 V or – 6 V to 6. The device is great for applications where the AC signals do not have a common mode voltage since both the positive and negative swing of the signal can be passed through the device with little distortion.

8.4 Device Functional Modes

表 8-1. Truth Table

IN	NC TO COM, COM TO NC	NO TO COM, COM TO NO
L	On	Off
H	Off	On

9 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Application Information

Analog signals that range over the entire supply voltage (V_{CC} to GND) or (V_{CC} to -V_{CC}) can be passed with very little change in ON-state resistance. The switches are bidirectional, so the NO, NC, and COM pins can be used as either inputs or outputs.

9.2 Typical Application

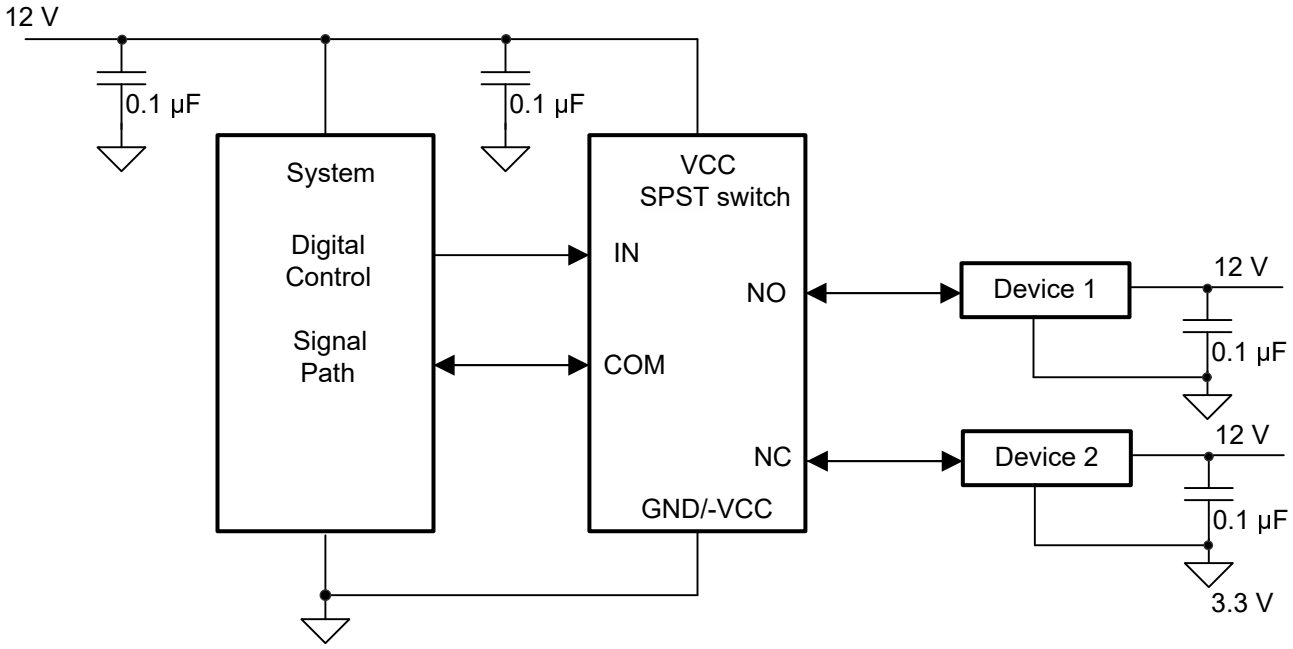


图 9-1. Typical Application Schematic

9.2.1 Design Requirements

Pull the digitally controlled input select pin IN to VCC or GND to avoid unwanted switch states that could result if the logic control pin is left floating.

9.2.2 Detailed Design Procedure

Select the appropriate supply voltage to cover the entire voltage swing of the signal passing through the switch since the TS12A12511 input or output signal swing of the device is dependant of the supply voltage V_{CC} and -V_{CC}.

9.2.3 Application Curve

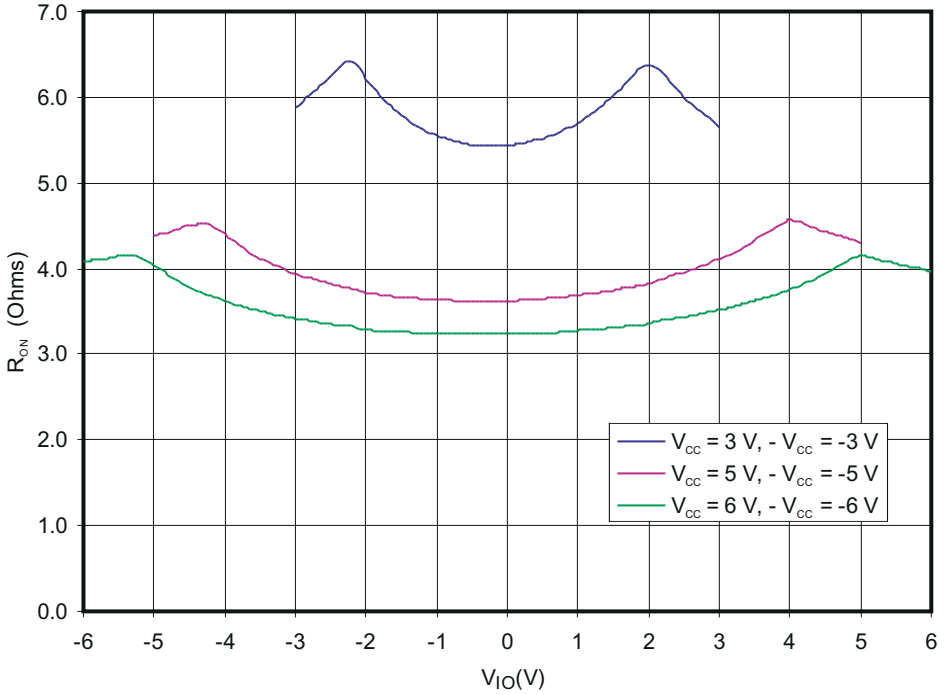


图 9-2. R_{ON} vs V_{IO}

10 Power Supply Recommendations

Proper power-supply sequencing is recommended for all CMOS devices. Do not exceed the absolute maximum ratings, because stresses beyond the listed ratings can cause permanent damage to the device. Always sequence VCC and -VCC on first, followed by NO, NC, or COM.

Although it is not required, power-supply bypassing improves noise margin and prevents switching noise propagation from the VCC supply to other components. A 0.1-μF capacitor, connected from VCC to GND, is adequate for most applications.

11 Layout

11.1 Layout Guidelines

It is recommended to place a bypass capacitor as close to the supply pins, VCC and -VCC, as possible to help smooth out lower frequency noise and provide better load regulation across the frequency spectrum. Minimize trace lengths and vias on the signal paths to preserve signal integrity.

11.2 Layout Example

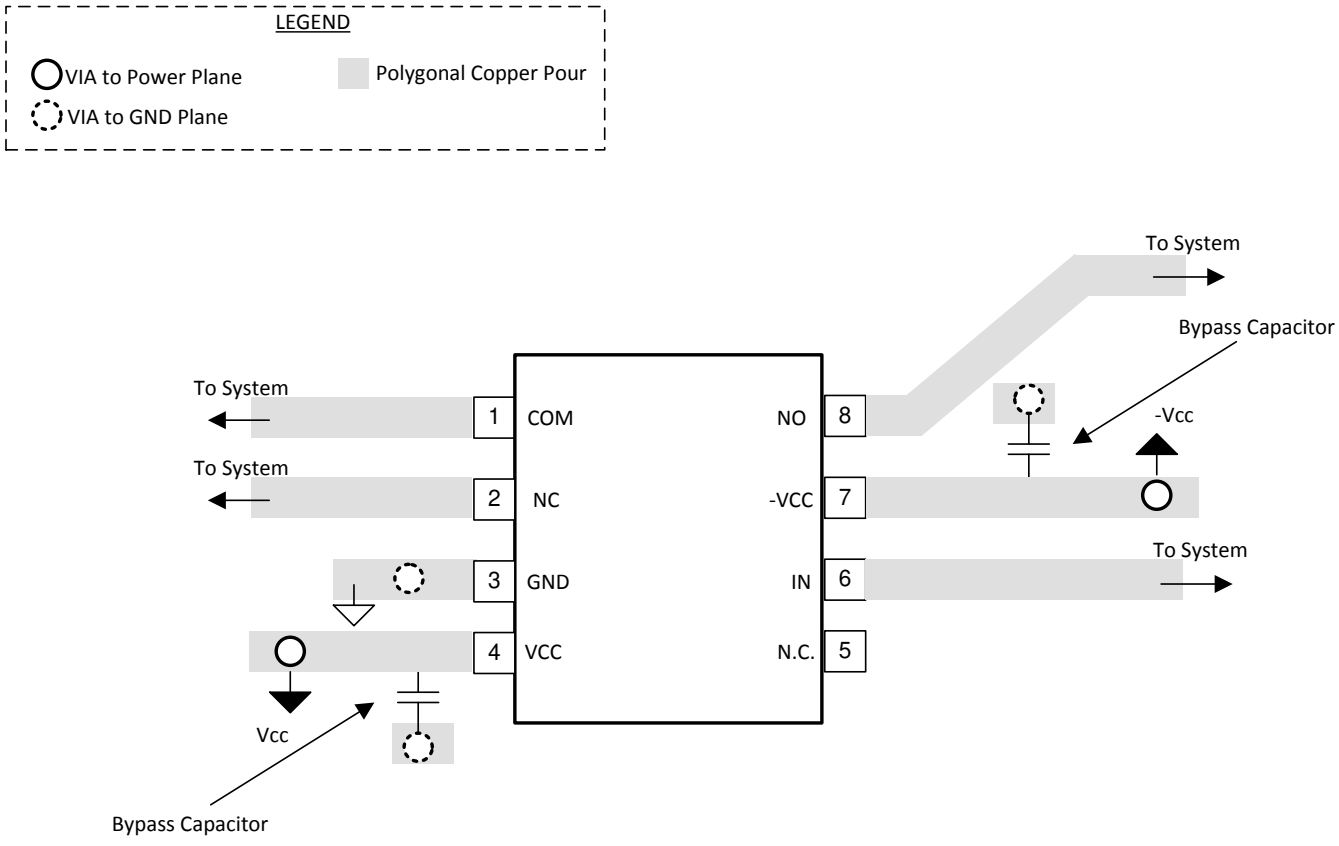


图 11-1. Layout Schematic

12 Device and Documentation Support

12.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.2 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

12.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TS12A12511DCNR	Active	Production	SOT-23 (DCN) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	NFHS NFHA
TS12A12511DCNR.A	Active	Production	SOT-23 (DCN) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	NFHS NFHA
TS12A12511DCNR.B	Active	Production	SOT-23 (DCN) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	NFHS NFHA
TS12A12511DGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2US 2UA
TS12A12511DGKR.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2US 2UA
TS12A12511DGKR.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2US 2UA
TS12A12511DRJR	Active	Production	SON (DRJ) | 8	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ZVE
TS12A12511DRJR.A	Active	Production	SON (DRJ) | 8	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ZVE
TS12A12511DRJR.B	Active	Production	SON (DRJ) | 8	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ZVE

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

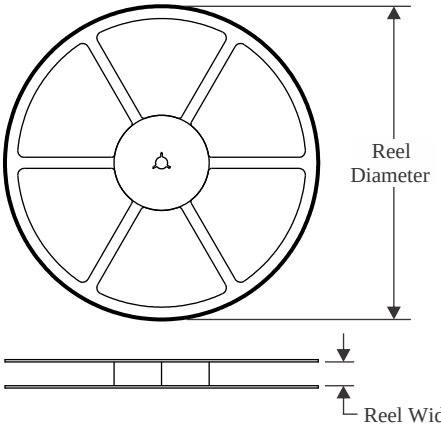
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

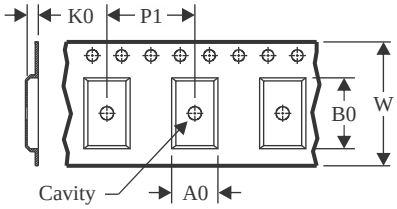
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

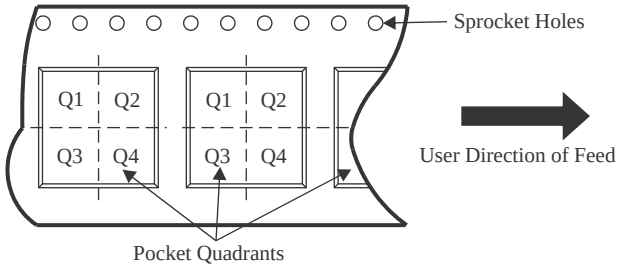


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

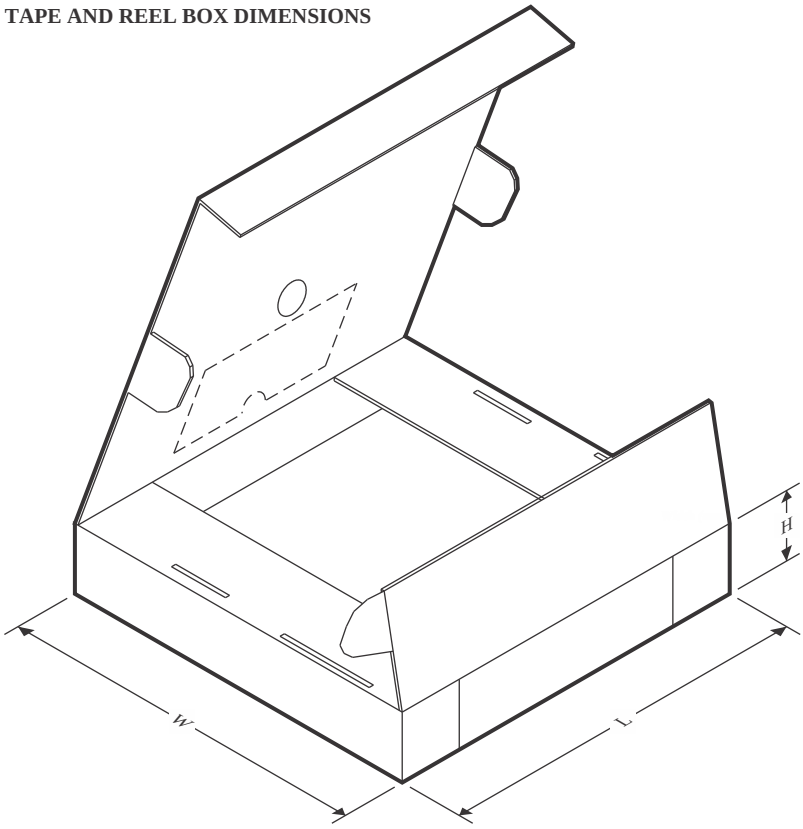
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS12A12511DCNR	SOT-23	DCN	8	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TS12A12511DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TS12A12511DRJR	SON	DRJ	8	1000	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

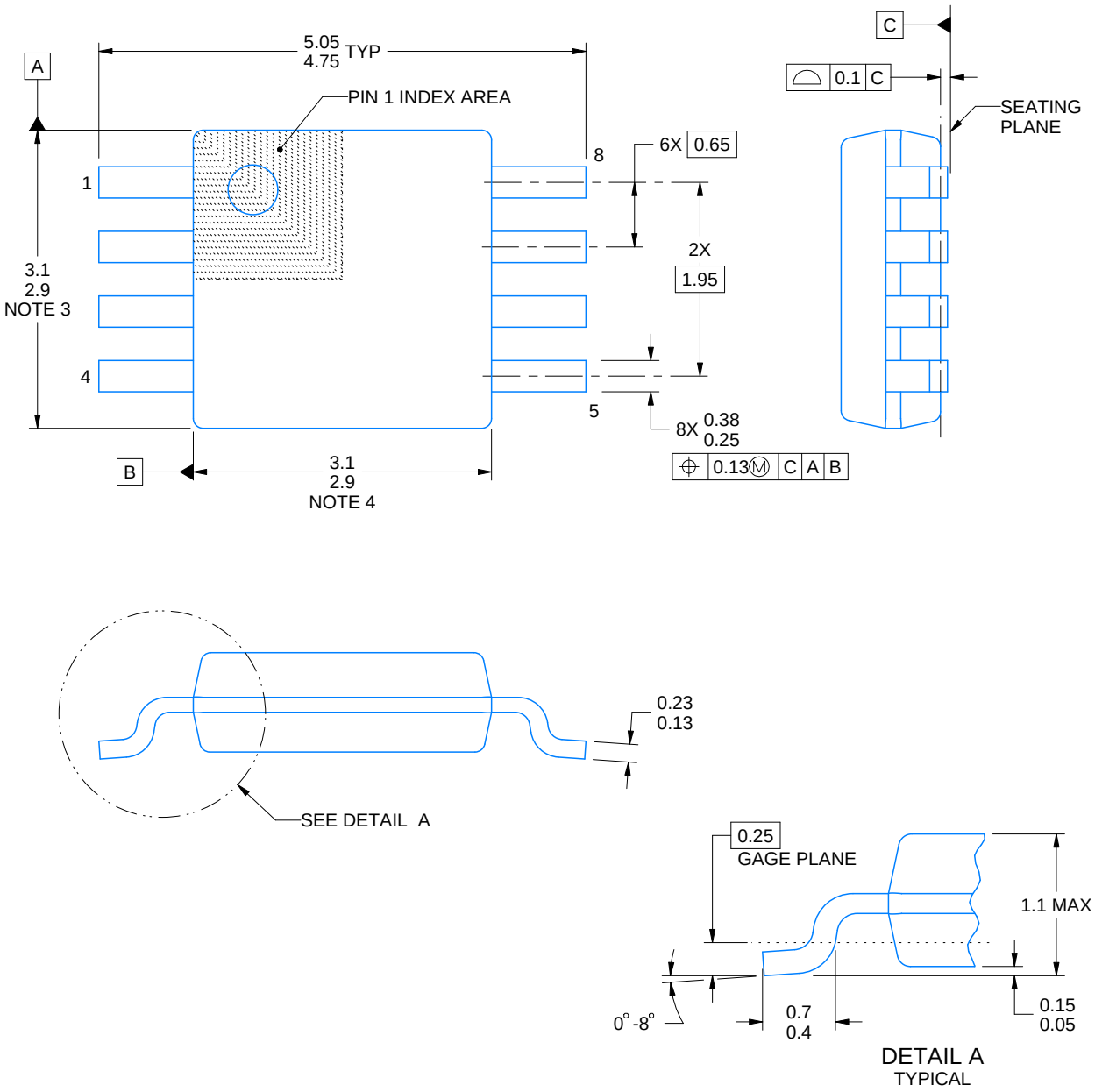
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS12A12511DCNR	SOT-23	DCN	8	3000	202.0	201.0	28.0
TS12A12511DGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
TS12A12511DRJR	SON	DRJ	8	1000	210.0	185.0	35.0

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

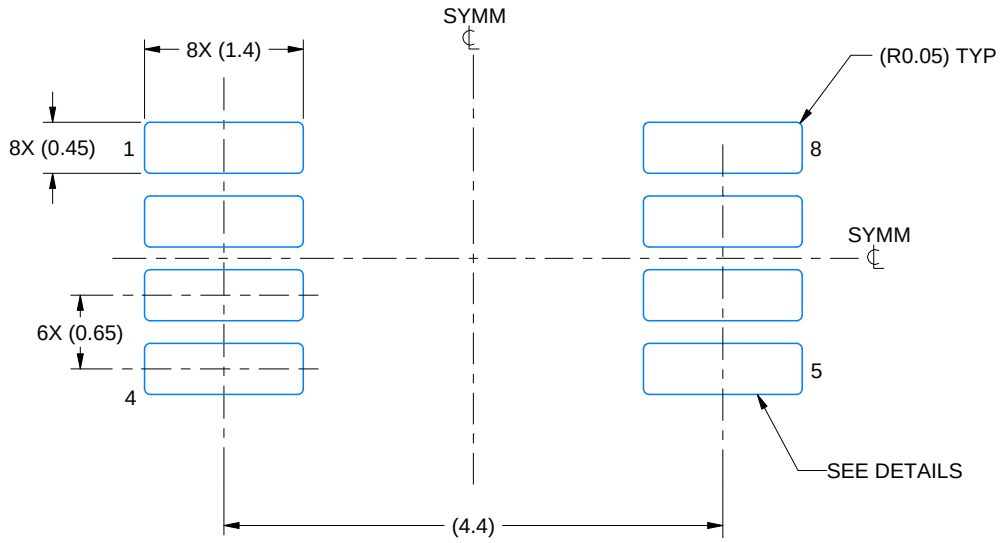
SMALL OUTLINE PACKAGE



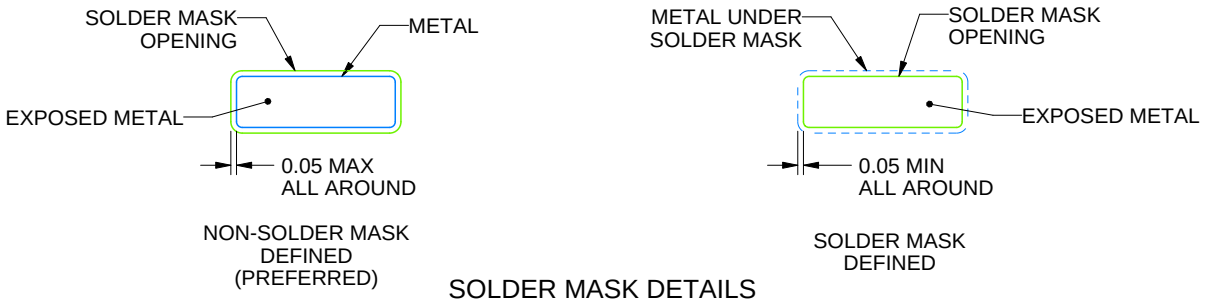
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

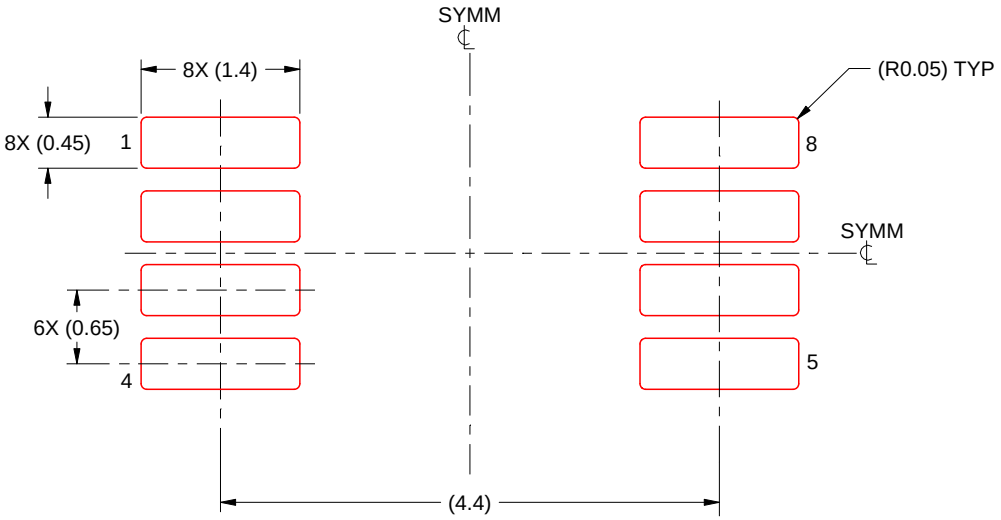


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



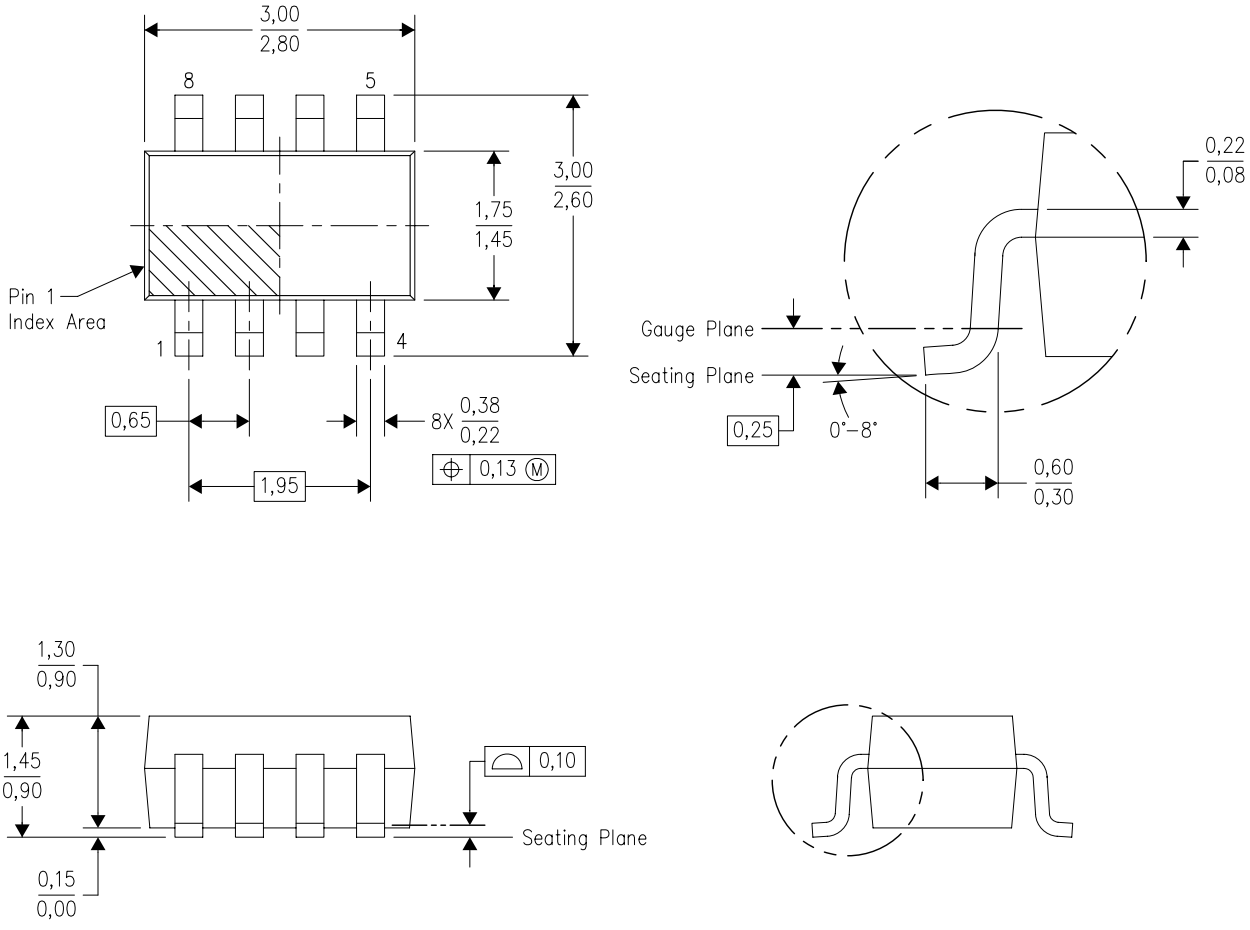
SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

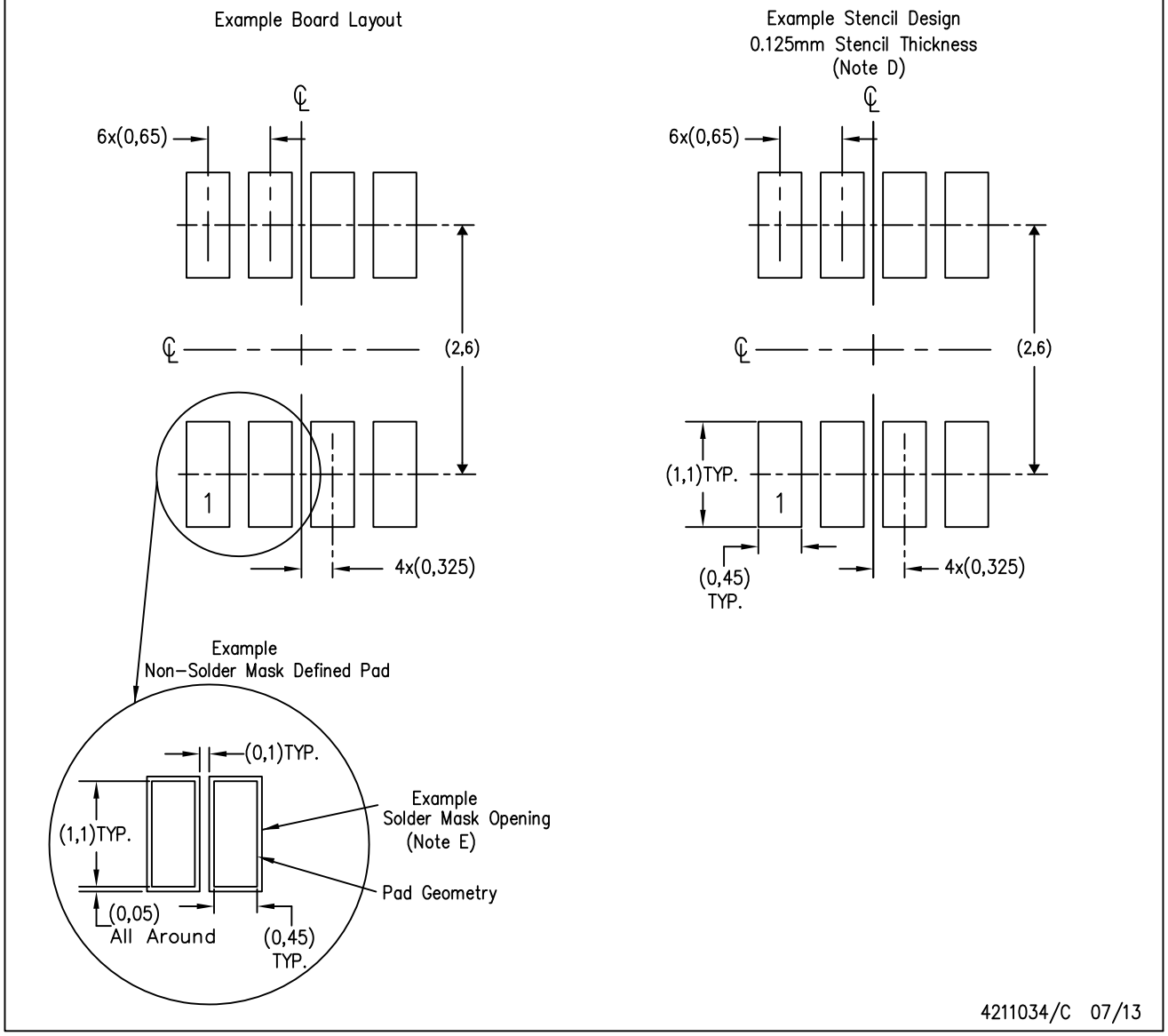
11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

DCN (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE (DIE DOWN)



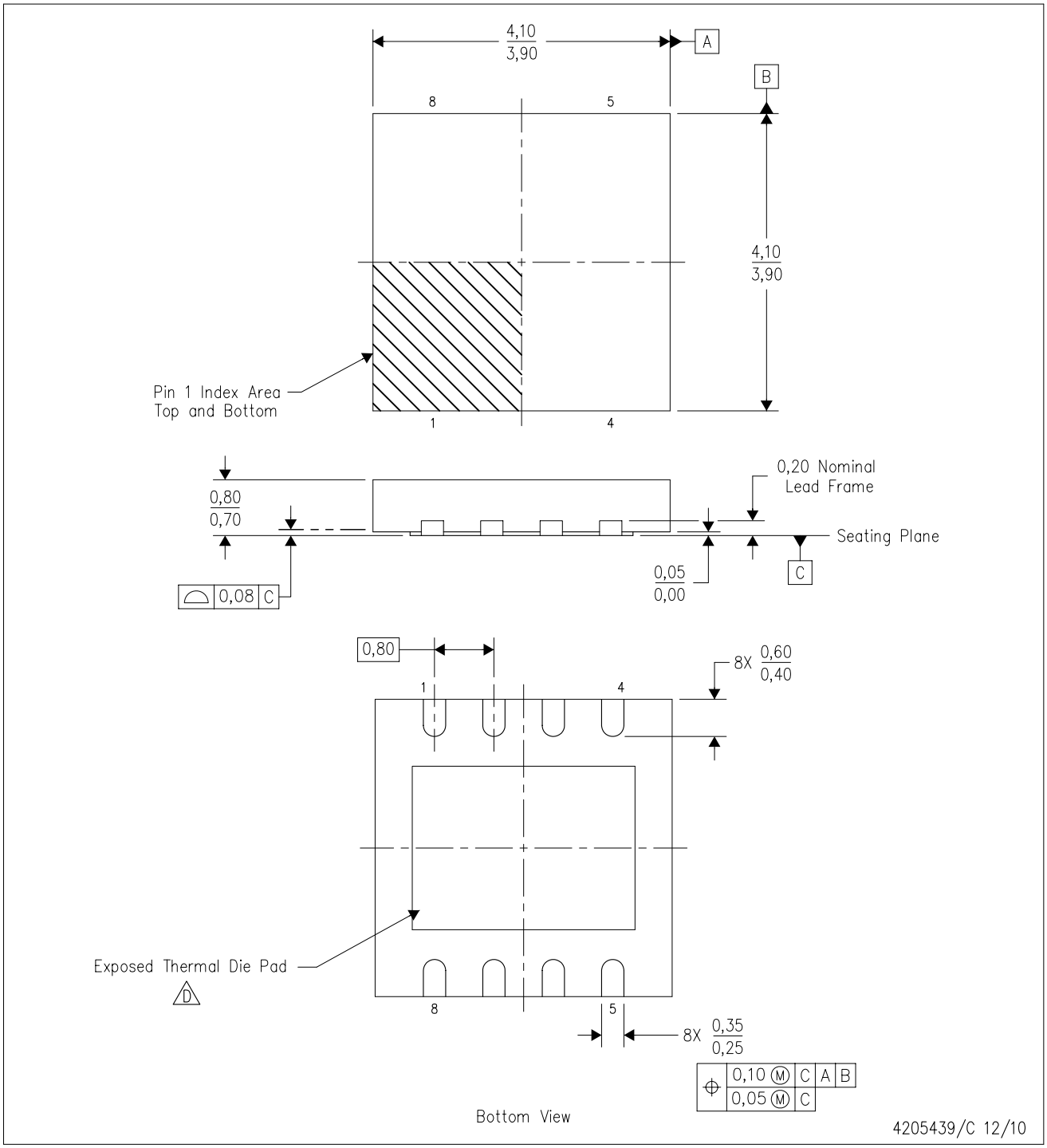
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Package outline exclusive of metal burr & dambar protrusion/intrusion.
D. Package outline inclusive of solder plating.
E. A visual index feature must be located within the Pin 1 index area.
F. Falls within JEDEC MO–178 Variation BA.
G. Body dimensions do not include flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.

DCN (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE (DIE DOWN)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DRJ (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Package complies to JEDEC MO–229 variation WGGB.

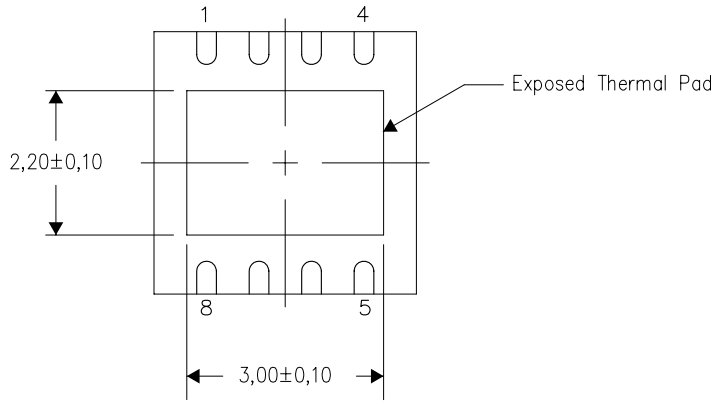
DRJ (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



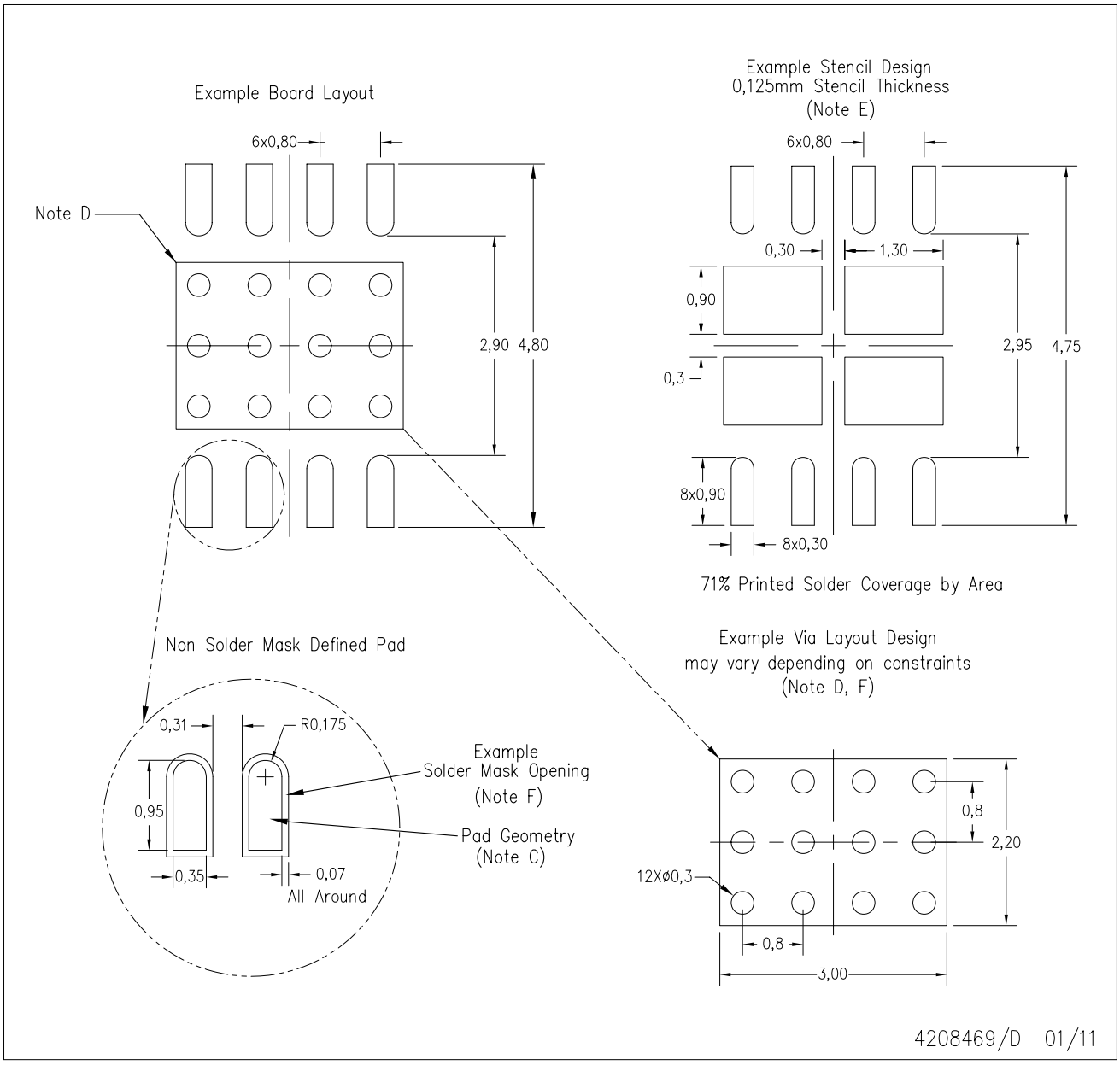
Bottom View

Exposed Thermal Pad Dimensions

4206882/F 01/11

NOTE: All linear dimensions are in millimeters

DRJ (S–PWSON–N8) SMALL PACKAGE OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with electropolish and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances and vias tenting recommendations for vias placed in the thermal pad.

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