



# PIC16F1826/1827

## 18-Pin 8-Bit Flash Microcontroller Product Brief

### High-Performance RISC CPU:

- Only 49 Instructions, including 14 new “C compiler-friendly” Instructions
- Operating Speed:
  - DC – 32 MHz clock input
  - DC – 125 ns instruction cycle
- Interrupt Capability with Automatic Context Saving
- 16-Level Deep Hardware Stack with Optional Overflow/Underflow Reset
- Direct, Indirect and Relative Addressing modes:
  - Two full 16-bit File Select Registers (FSRs)
  - FSRs can read program and data memory

### Special Microcontroller Features:

- Precision Internal Oscillator:
  - Factory calibrated to  $\pm 1\%$ , typical
  - Software selectable frequency range from 32 MHz to 31 kHz
- 31 kHz Low-Power Internal Oscillator
- External Oscillator Block with:
  - 4 crystal/resonator modes up to 32 MHz using 4xPLL
  - 3 external clock modes up to 32 MHz
- 4x Phase Locked Loop (PLL)
- Fail-Safe Clock Monitor
- Two-Speed Start-up
- Power-Saving Sleep mode
- Power-on Reset (POR)
- Power-up Timer (PWRT)
- Oscillator Start-up Timer (OST)
- Brown-out Reset (BOR) with Selectable Trip Point
- Extended Watch-Dog Timer (WDT)
- In-Circuit Serial Programming™ (ICSP™)
- In-Circuit Debug (ICD)
- Enhanced Low-Voltage Programming (LVP)
- Operating Voltage Range:
  - 1.8V to 3.6V (PIC16LF182X)
  - 1.8V to 5.5V (PIC16F182x)
- Programmable Code Protection
- Self-Programmable under Software Control

### Low-Power Features:

- Standby Current (PIC16LF182X):
  - 100 nA @ 1.8V, typical
- Operating Current (PIC16LF182X):
  - 150  $\mu$ A @ 1 MHz, 1.8V, typical
- Low-Power Watchdog Timer Current (PIC16LF182X):
  - 1.0  $\mu$ A @ 1.8V, typical

### Peripheral Features:

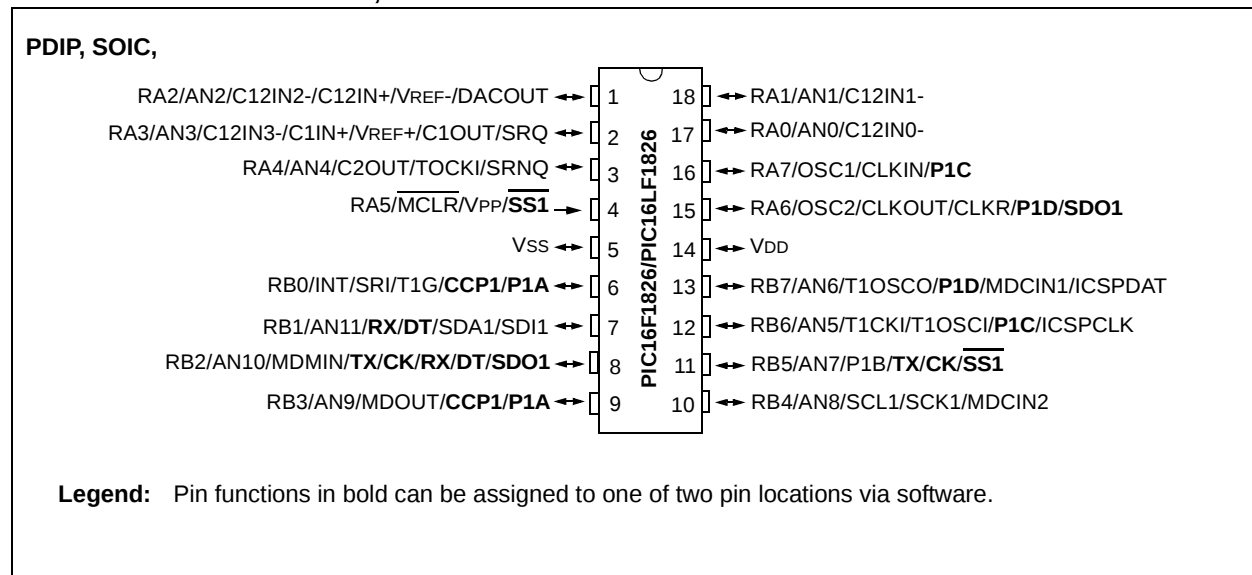
- Up to 15 I/O Pins and 1 Input-only Pin:
  - High current sink/source for LED drivers
  - Individually programmable interrupt-on-change pins
  - Individually programmable weak pull-ups
- Timer0: 8-Bit Timer/Counter with 8-Bit Programmable Prescaler
- Enhanced Timer1:
  - 16-bit timer/counter with prescaler
  - External Gate Input mode
  - Dedicated low-power 32 kHz oscillator driver
- Timer2, 4, 6: 8-Bit Timer/Counter with 8-Bit Period Register, Prescaler and Postscaler
- Up to two Enhanced Capture, Compare, PWM modules (ECCP):
  - Software selectable time bases
  - Auto-shutdown and auto-restart
  - PWM steering
- Up to two Capture/Compare/PWM modules (CCP):
  - Software selectable time bases
- Up to two Master Synchronous Serial Port (MSSP) with SPI and I<sup>2</sup>C™ with:
  - 7-bit address masking
  - SMBus/PMBus™ compatibility
- Enhanced Universal Synchronous Asynchronous Receiver Transmitter (EUSART):
  - RS-232, RS-485 and LIN compatible
  - Auto-Baud Detect
  - Auto-wake-up on start
- SR Latch (Integrated 555 Timer):
  - Multiple Set/Reset input options
- Analog-to-Digital Converter (ADC):
  - 10-bit resolution
  - Up to 12 channels
- 2 Comparators:
  - Rail-to-rail inputs
  - Power mode control
  - Software controllable hysteresis
- Voltage Reference module:
  - Fixed Voltage Reference (FVR) with 1.024V, 2.048V and 4.096V output levels
  - 5-bit rail-to-rail resistive DAC with positive and negative reference selection
- mTouch™ Sensing oscillator module
  - Up to 12 channels for button, sensor or slider input
- Data Signal Modulator module
  - Select modulator and carrier sources from various module outputs

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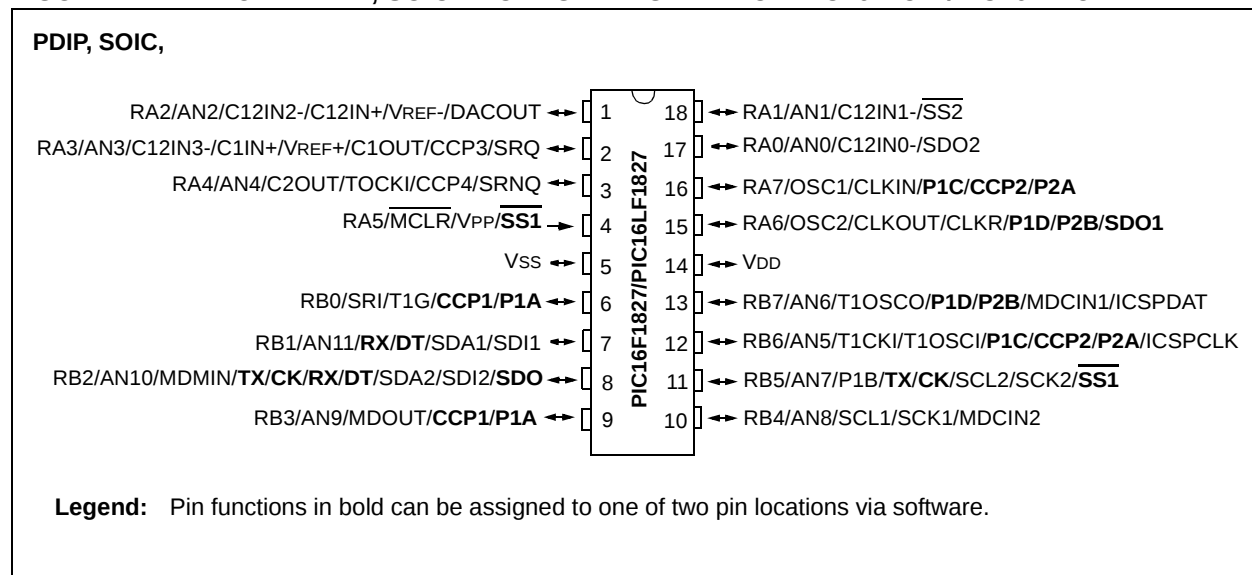
**TABLE 1: PIC16F1826/1827/PIC16LF1826/1827 FAMILY TYPES**

| Device      | Program Memory Flash (words) | Data EEPROM (bytes) | SRAM (bytes) | I/Os | 10-bit A/D (ch) | Timers 8/16-bit | EUSART | MSSP | CCP/ ECCP | Cap Touch Channels |
|-------------|------------------------------|---------------------|--------------|------|-----------------|-----------------|--------|------|-----------|--------------------|
| PIC16F1826  | 2048                         | 256                 | 256          | 16   | 12              | 2/1             | Yes    | 1    | 0/1       | 12                 |
| PIC16LF1826 | 2048                         | 256                 | 256          | 16   | 12              | 2/1             | Yes    | 1    | 0/1       | 12                 |
| PIC16F1827  | 4096                         | 256                 | 384          | 16   | 12              | 4/1             | Yes    | 2    | 2/2       | 12                 |
| PIC16LF1827 | 4096                         | 256                 | 384          | 16   | 12              | 4/1             | Yes    | 2    | 2/2       | 12                 |

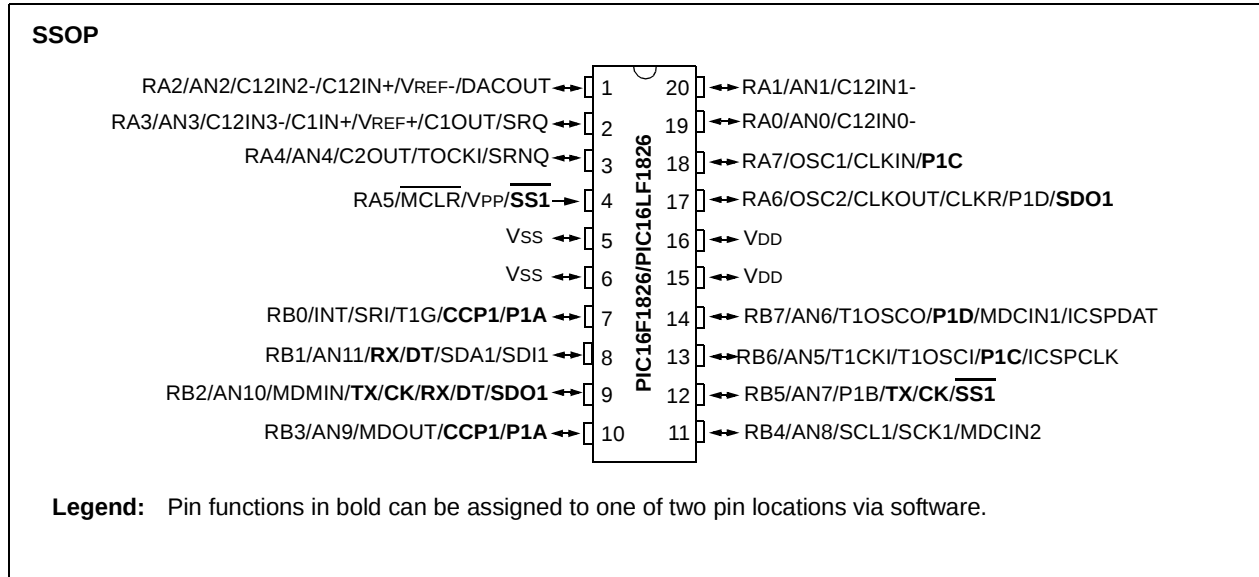
**FIGURE 1: 18-PIN PDIP, SOIC PACKAGE DIAGRAM FOR PIC16F1826/PIC16LF1826**



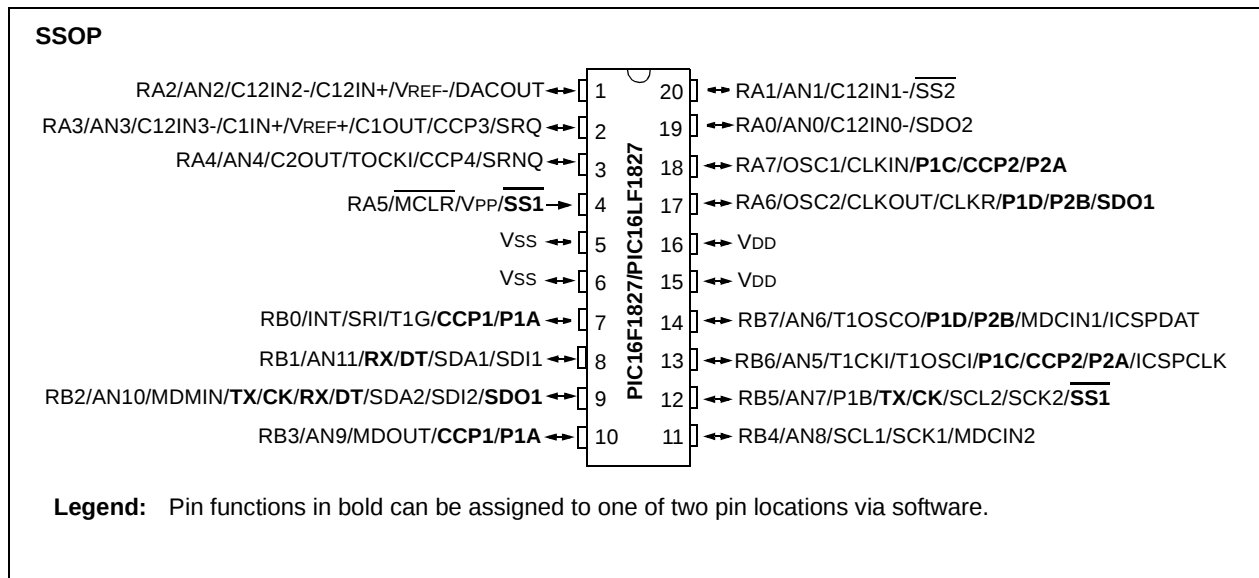
**FIGURE 2: 18-PIN PDIP, SOIC PACKAGE DIAGRAM FOR PIC16F1827/PIC16LF1827**



**FIGURE 3: 20-PIN SSOP PACKAGE DIAGRAM FOR PIC16F1826/PIC16LF1826**



**FIGURE 4: 20-PIN SSOP PACKAGE DIAGRAM FOR PIC16F1827/PIC16LF1827**



**FIGURE 5: 28-PIN QFN PACKAGE DIAGRAM FOR PIC16F1826**

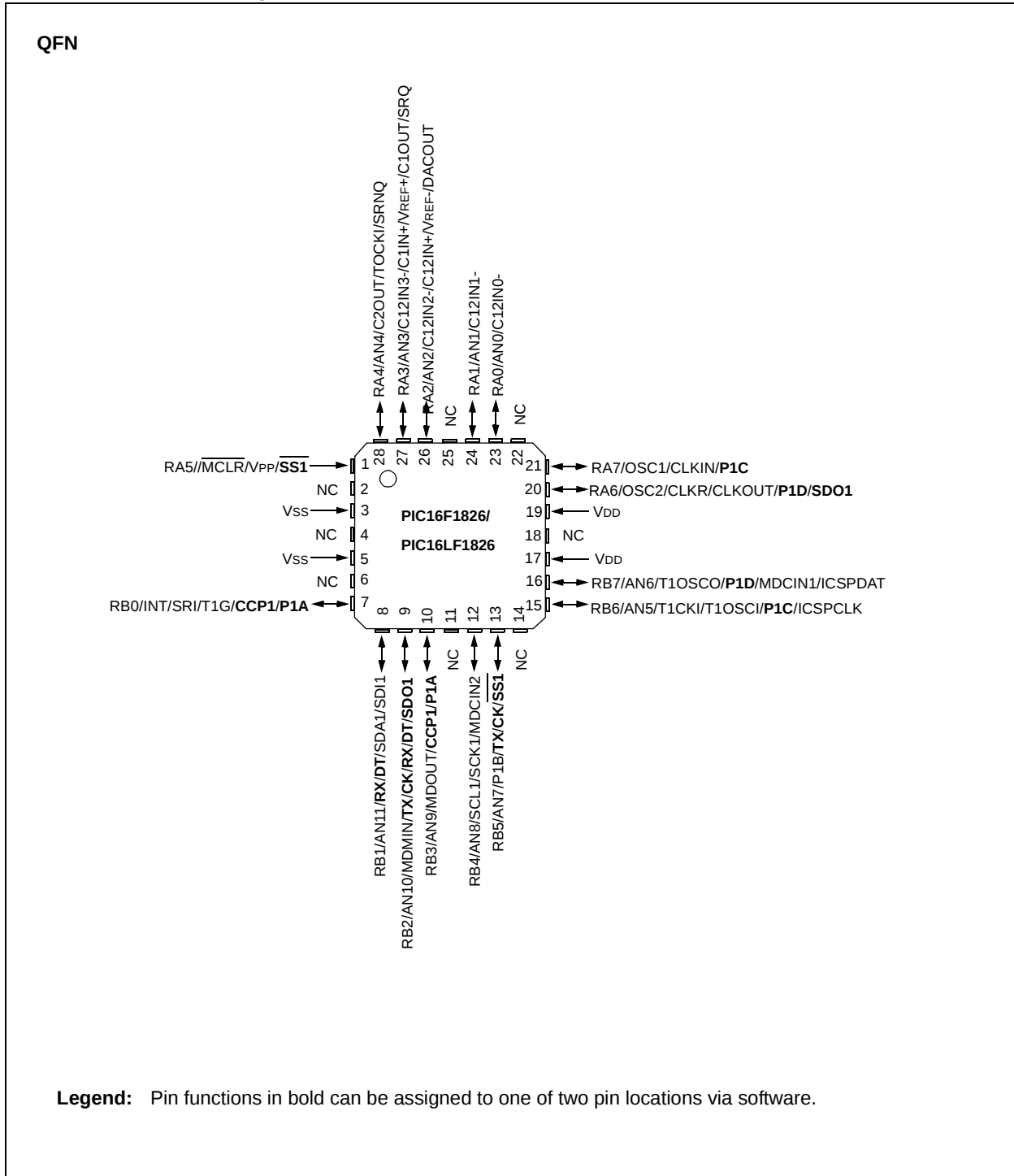
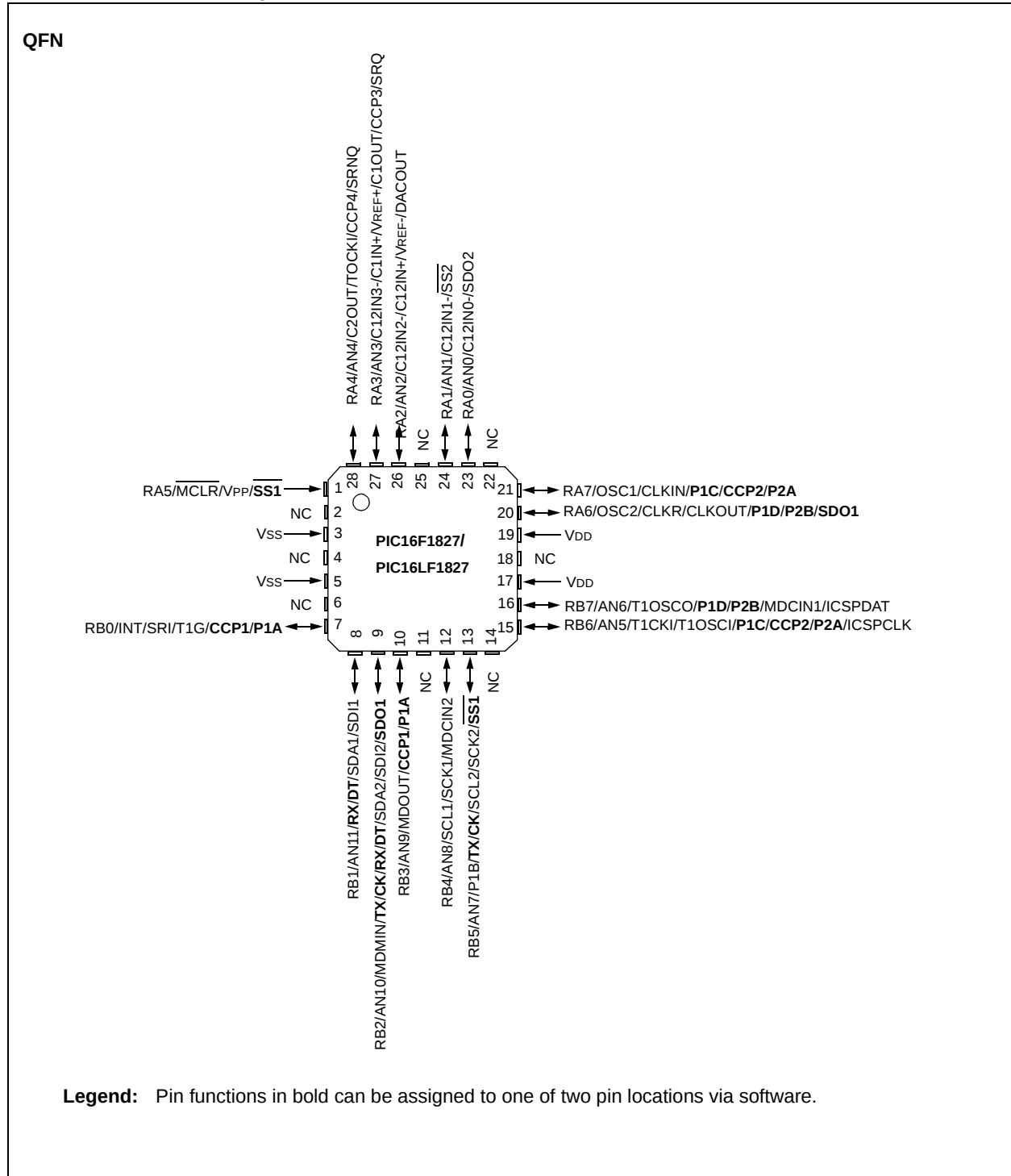


FIGURE 6: 28-PIN QFN PACKAGE DIAGRAM FOR PIC16F1827



# PIC16F1826/1827

**TABLE 2: PIN ALLOCATION TABLE (PIC16F1826/1827)**

| I/O | 18-Pin PDIP/SOIC | 20-Pin SSOP | 28-Pin QFN | A/D  | Cap Sense | Comparator            | SR Latch | Timers          | CCP                                                                 | EUSART                                                                           | MSSP                                                              | Interrupt  | Modulator | Pull-up | Basic                  |
|-----|------------------|-------------|------------|------|-----------|-----------------------|----------|-----------------|---------------------------------------------------------------------|----------------------------------------------------------------------------------|-------------------------------------------------------------------|------------|-----------|---------|------------------------|
| RA0 | 17               | 19          | 23         | AN0  | CPS0      | C12IN0-               | —        | —               | —                                                                   | —                                                                                | SDO2 <sup>(2)</sup>                                               | —          | —         | N       | —                      |
| RA1 | 18               | 20          | 24         | AN1  | CPS1      | C12IN1-               | —        | —               | —                                                                   | —                                                                                | SS2 <sup>(2)</sup>                                                | —          | —         | N       | —                      |
| RA2 | 1                | 1           | 26         | AN2  | CPS2      | C12IN2-C12IN+         | —        | —               | —                                                                   | —                                                                                | —                                                                 | —          | —         | N       | DACOUT<br>VREF-        |
| RA3 | 2                | 2           | 27         | AN3  | CPS3      | C12IN3-C1IN+<br>C1OUT | SRQ      | —               | CCP3 <sup>(2)</sup>                                                 | —                                                                                | —                                                                 | —          | —         | N       | VREF+                  |
| RA4 | 3                | 3           | 28         | AN4  | CPS4      | C2OUT                 | SRNQ     | T0CKI           | CCP4 <sup>(2)</sup>                                                 | —                                                                                | —                                                                 | —          | —         | N       | —                      |
| RA5 | 4                | 4           | 1          | —    | —         | —                     | —        | —               | —                                                                   | —                                                                                | SS1 <sup>(1)</sup>                                                | —          | —         | Y       | MCLR<br>VPP            |
| RA6 | 15               | 17          | 20         | —    | —         | —                     | —        | —               | P1D <sup>(1)</sup><br>P2B <sup>(1,2)</sup>                          | —                                                                                | SDO1 <sup>(1)</sup>                                               | —          | —         | N       | OSC2<br>CLKOUT<br>CLKR |
| RA7 | 16               | 18          | 21         | —    | —         | —                     | —        | —               | P1C <sup>(1)</sup><br>CCP2 <sup>(1,2)</sup><br>P2A <sup>(1,2)</sup> | —                                                                                | —                                                                 | —          | —         | N       | OSC1<br>CLKIN          |
| RB0 | 6                | 7           | 7          | —    | —         | —                     | SRI      | T1G             | CCP1 <sup>(1)</sup><br>P1A <sup>(1)</sup>                           | —                                                                                | —                                                                 | INT<br>IOC | —         | Y       | —                      |
| RB1 | 7                | 8           | 8          | AN11 | CPS11     | —                     | —        | —               | —                                                                   | RX <sup>(1)</sup><br>DT <sup>(1)</sup>                                           | SDA1<br>SDI1                                                      | IOC        | —         | Y       | —                      |
| RB2 | 8                | 9           | 9          | AN10 | CPS10     | —                     | —        | —               | —                                                                   | RX <sup>(1)</sup><br>DT <sup>(1)</sup><br>TX <sup>(1)</sup><br>CK <sup>(1)</sup> | SDA2 <sup>(2)</sup><br>SDI2 <sup>(2)</sup><br>SDO1 <sup>(1)</sup> | IOC        | MDMIN     | Y       | —                      |
| RB3 | 9                | 10          | 10         | AN9  | CPS9      | —                     | —        | —               | CCP1 <sup>(1)</sup><br>P1A <sup>(1)</sup>                           | —                                                                                | —                                                                 | IOC        | MDOUT     | Y       | —                      |
| RB4 | 10               | 11          | 12         | AN8  | CPS8      | —                     | —        | —               | —                                                                   | —                                                                                | SCL1<br>SCK1                                                      | IOC        | MDCIN2    | Y       | —                      |
| RB5 | 11               | 12          | 13         | AN7  | CPS7      | —                     | —        | —               | P1B                                                                 | TX <sup>(1)</sup><br>CK <sup>(1)</sup>                                           | SCL2 <sup>(2)</sup><br>SCK2 <sup>(2)</sup><br>SS1 <sup>(1)</sup>  | IOC        | —         | Y       | —                      |
| RB6 | 12               | 13          | 15         | AN5  | CPS5      | —                     | —        | T1CKI<br>T1OSCI | P1C <sup>(1)</sup><br>CCP2 <sup>(1,2)</sup><br>P2A <sup>(1,2)</sup> | —                                                                                | —                                                                 | IOC        | —         | Y       | ICSPCLK                |
| RB7 | 13               | 14          | 16         | AN6  | CPS6      | —                     | —        | T1OSCO          | P1D <sup>(1)</sup><br>P2B <sup>(1,2)</sup>                          | —                                                                                | —                                                                 | IOC        | MDCIN1    | Y       | ICSPDAT                |
| VDD | 14               | 15,<br>16   | 17,<br>19  | —    | —         | —                     | —        | —               | —                                                                   | —                                                                                | —                                                                 | —          | —         | —       | VDD                    |
| VSS | 5                | 5,<br>6     | 3,<br>5    | —    | —         | —                     | —        | —               | —                                                                   | —                                                                                | —                                                                 | —          | —         | —       | VSS                    |

**Note 1:** Pin functions can be assigned to one of two pin locations via software.

**2:** Functions are only available on the PIC16F1827 and PIC16LF1827.

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