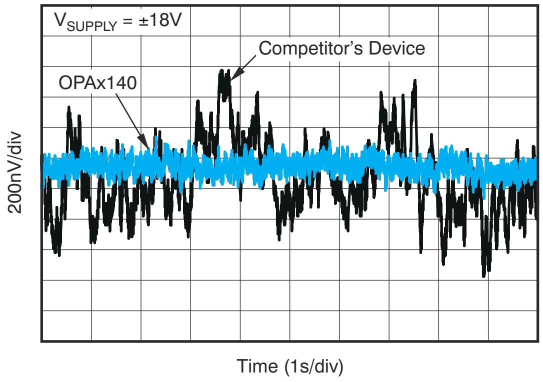
OPAx140 高精度、低噪声、轨至轨输出、11MHz JFET 运算放大器

1 特性

- 非常低的温漂：1 μV/°C（最大值）
- 极低的偏移：120 μV
- 低输入偏置电流：10 pA（最大值）
- 超低的 1/f 噪声：$250nV_{PP}$（0.1Hz 至 10Hz）
- 低噪声：5.1 nV/√Hz
- 压摆率：20 V/μs
- 低电源电流：2 mA（最大值）
- 输入电压范围包括 V– 电源
- 单电源运行：4.5V 至 36V
- 双电源供电：±2.25V 至 ±18V
- 无相位反转
- 封装：
  - 业界通用 SOIC、SON、SOT-23、TSSOP 和 VSSOP

2 应用

- 数据中心内部互联（地铁）
- 半导体测试
- 化学和气体分析仪
- 直流电源、交流电源、电子负载
- 数据采集 (DAQ)
- 实验室和现场仪表



0.1Hz 至 10Hz 噪声

3 说明

OPA140、OPA2140 和 OPA4140 (OPAx140) 运算放大器 (op amp) 系列是一系列具有良好漂移和低输入偏置电流的低功耗 JFET 输入放大器。凭借其包括 V- 在内的轨到轨输出摆幅和输入范围，设计人员可以利用 JFET 放大器的低噪声特性，同时还可以连接到现代单电源精密模数转换器 (ADC) 和数模转换器 (DAC)。

OPA140 可实现 11MHz 单位增益带宽和 20V/μs 压摆率，同时仅消耗 1.8mA（典型值）的静态电流。该器件由 4.5V 至 36V 单电源或 ±2.25V 至 ±18V 双电源供电。

所有器件版本的额定工作温度范围均为 –40°C 至 +125°C，可用于最具有挑战性的环境中。OPA140（单通道）采用 5 引脚 SOT-23、8 引脚 VSSOP 和 8 引脚 SOIC 封装。OPA2140（双通道）采用 8 引脚 SON、8 引脚 VSSOP 和 8 引脚 SOIC 封装。OPA4140（四通道）采用 14 引脚 SOIC 和 14 引脚 TSSOP 封装。

器件信息

器件型号	通道	封装(1)
OPA140	单通道	D（SOIC，8）
		DBV（SOT23，5）
		DGK（VSSOP，8）
OPA2140	双通道	D（SOIC，8）
		DRG（SON，8）
		DGK（VSSOP，8）
OPA4140	四通道	D（SOIC，14）
		PW（TSSOP，14）

(1) 如需了解所有可用封装，请参阅数据表末尾的封装选项附录。

Table of Contents

1 特性.......... 1
2 应用.......... 1
3 说明.......... 1
4 Revision History.......... 2
5 Pin Configuration and Functions.......... 3
6 Specifications.......... 5
  6.1 Absolute Maximum Ratings.......... 5
  6.2 ESD Ratings.......... 5
  6.3 Recommended Operating Conditions.......... 5
  6.4 Thermal Information: OPA140.......... 6
  6.5 Thermal Information: OPA2140.......... 6
  6.6 Thermal Information: OPA4140.......... 6
  6.7 Electrical Characteristics.......... 7
  6.8 Typical Characteristics.......... 8
7 Detailed Description.......... 15
  7.1 Overview.......... 15
  7.2 Functional Block Diagram.......... 15
  7.3 Feature Description.......... 15
  7.4 Device Functional Modes.......... 23
8 Application and Implementation.......... 24
  8.1 Application Information.......... 24
  8.2 Typical Application.......... 24
  8.3 Power Supply Recommendations.......... 25
  8.4 Layout.......... 25
9 Device and Documentation Support.......... 28
  9.1 Device Support.......... 28
  9.2 Documentation Support.......... 29
  9.3 接收文档更新通知.......... 29
  9.4 支持资源.......... 29
  9.5 Trademarks.......... 29
  9.6 静电放电警告.......... 29
  9.7 术语表.......... 29
10 Mechanical, Packaging, and Orderable Information.......... 29

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision E (July 2021) to Revision F (March 2023) **Page**

- 将 OPA2140 DRG 封装从“预发布”更改为“量产数据”.......... 1
- Added ± to input offset voltage and input offset voltage drift values in the *Electrical Characteristics*.......... 7
- Changed 12-bit settling time specification unit from ns to µs in the *Electrical Characteristics*.......... 7
- Deleted incorrect power supply voltage parameter from the *Electrical Characteristics* and moved corrected values to the *Recommended Operating Conditions*.......... 7
- Added thermal-related information to the OPA2140 DRG package in the *Thermal Protection* section.......... 18
- Changed Figure 7-3 and Figure 7-4 for clarity.......... 18
- Changed Figure 8-3, *Dual Operational Amplifier Board Layout for Noninverting Configuration* to show the dual DRG package option.......... 27

Changes from Revision D (January 2019) to Revision E (July 2021) **Page**

- 向数据表添加了 OPA2140 DRG 预发布封装和相关内容.......... 1

Changes from Revision C (August 2016) to Revision D (January 2019) **Page**

- Changed Figure 12 x-axis title From: Frequency (Hz) To: Output Amplitude (V_{RMS}).......... 8

Changes from Revision B (November 2015) to Revision C (August 2016) **Page**

- Changed units for E_n Input voltage noise From: µV To: nV in Electrical Characteristics: V_S = 4.5 V to 36 V; ±2.25 V to ±18 V.......... 7

Changes from Revision A (August 2010) to Revision B (November 2015) **Page**

- 添加了 *ESD 等级* 表、*特性说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源相关建议* 部分、*布局* 部分、*器件和文档支持* 部分以及 *机械、封装和可订购信息* 部分.......... 1
- Changed title of 表 6-1 From: *Characteristic Performance Measurements* To: *Table of Graphs*.......... 8
- Changed section 7.37 title From: *Power Dissipation and Thermal Protection* To: *Thermal Protection*.......... 18

5 Pin Configuration and Functions

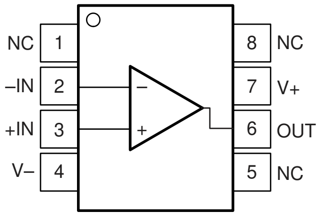


图 5-1. OPA140: D Package, 8-Pin SOIC and DGK Package, 8-Pin VSSOP (Top View)

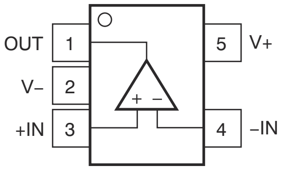


图 5-2. OPA140: DBV Package, 5-Pin SOT-23 (Top View)

表 5-1. Pin Functions: OPA140

PIN			TYPE	DESCRIPTION
NAME	OPA140			
	D (SOIC), DGK (VSSOP)	DBV (SOT)		
+IN	3	3	Input	Noninverting input
–IN	2	4	Input	Inverting input
NC	1, 5, 8	—	—	No internal connection (can be left floating)
OUT	6	1	Output	Output
V+	7	5	—	Positive (highest) power supply
V–	4	2	—	Negative (lowest) power supply

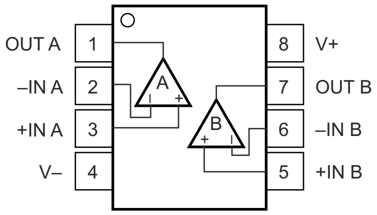


图 5-3. OPA2140: D Package, 8-Pin SOIC and DGK Package, 8-Pin VSSOP (Top View)

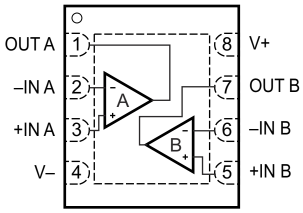


图 5-4. OPA2140: DRG Package, 8-Pin SON (Top View)

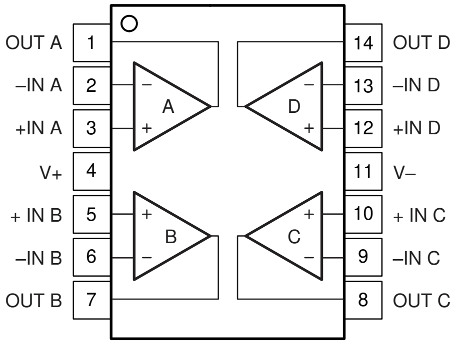


图 5-5. OPA4140: D Package, 14-Pin SOIC and PW Package, 14-Pin TSSOP (Top View)

表 5-2. Pin Functions: OPA2140 and OPA4140

PIN			TYPE	DESCRIPTION
NAME	OPA2140 D (SOIC), DGK (VSSOP), DRG (SON)	OPA4140 D (SOIC), PW (TSSOP)		
+IN A	3	3	Input	Noninverting input, channel A
+IN B	5	5	Input	Noninverting input, channel B
+IN C	—	10	Input	Noninverting input, channel C
+IN D	—	12	Input	Noninverting input, channel D
–IN A	2	2	Input	Inverting input, channel A
–IN B	6	6	Input	Inverting input, channel B
–IN C	—	9	Input	Inverting input, channel C
–IN D	—	13	Input	Inverting input, channel D
OUT A	1	1	Output	Output, channel A
OUT B	7	7	Output	Output, channel B
OUT C	—	8	Output	Output, channel C
OUT D	—	14	Output	Output, channel D
V+	8	4	—	Positive (highest) power supply
V–	4	11	—	Negative (lowest) power supply
Thermal Pad	DRG Package only	—	—	Thermal pad is internally connected to V−. Solder the thermal pad to a heat spreading plane on the board connected to V−. For DRG package only.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_S	Supply voltage, (V+) – (V–)	Dual supply		±20	V
		Single supply		40	
	Signal input pins(2)	Voltage	(V–) – 0.5	(V+) + 0.5	V
		Current		±10	mA
	Output short-circuit(3)		Continuous		
T_A	Ambient temperature		–55	150	°C
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Input pins are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails must be current limited to 10 mA or less.

(3) Short-circuit to V_S / 2 (ground in symmetrical dual-supply setups), one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_S	Supply voltage, (V+) – (V–)	Dual supply	±2.25		±18	V
		Single supply	4.5		36	
T_A	Ambient temperature		–40		125	°C

6.4 Thermal Information: OPA140

THERMAL METRIC (1)		OPA140			UNIT
		D (SOIC)	DBV (SOT)	DGK (VSSOP)	
		8 PINS	5 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	160	210	180	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	75	200	55	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	60	110	130	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	9	40	N/A	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	50	105	120	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Thermal Information: OPA2140

THERMAL METRIC (1)		OPA2140			UNIT
		D (SOIC)	DGK (VSSOP)	DRG (SON)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	160	180	50.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	75	55	50.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	60	130	23.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	9	N/A	0.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	50	120	23.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	7.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.6 Thermal Information: OPA4140

THERMAL METRIC (1)		OPA4140		UNIT
		D (SOIC)	PW (TSSOP)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	97	135	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	56	45	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	53	66	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	19	N/A	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	46	60	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.7 Electrical Characteristics

at T_A = 25°C, V_S = 4.5 V (±2.25) to 36 V (±18 V), R_L = 2 kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage				±30	±120	µV
		V_S = ±18 V, T_A = –40°C to +125°C				±220	
		V_S = ±2.25 V to ±18 V, T_A = –40°C to +125°C				±4	µV/V
dV_{OS}/dT	Input offset voltage drift	V_S = ±18 V, T_A = –40°C to +125°C			±0.35	±1	µV/°C
PSRR	Power-supply rejection ratio	V_S = ±2.25 V to ±18 V, T_A = –40°C to +125°C			±0.1	±0.5	µV/V
INPUT BIAS CURRENT							
I_B	Input bias current				±0.5	±10	pA
		T_A = –40°C to +125°C				±3	nA
I_{OS}	Input offset current				±0.5	±10	pA
		T_A = –40°C to +125°C				±1	nA
NOISE							
E_n	Input voltage noise	f = 0.1 Hz to 10 Hz			250		nV_{PP}
		f = 0.1 Hz to 10 Hz			42		nV_{RMS}
e_n	Input voltage noise density	f = 10 Hz			8		nV/√Hz
		f = 100 Hz			5.8		
		f = 1 kHz			5.1		
I_n	Input current noise density	f = 1 kHz			0.8		fA/√Hz
INPUT VOLTAGE RANGE							
V_{CM}	Common-mode voltage	T_A = –40°C to +125°C		(V–) – 0.1		(V+) – 3.5	V
CMRR	Common-mode rejection ratio	V_S = ±18 V, V_{CM} = (V–) – 0.1 V to (V+) – 3.5 V		126	140		dB
			T_A = –40°C to +125°C	120			
INPUT IMPEDANCE							
Z_{ID}	Differential				10^{13} || 10		Ω || pF
Z_{IC}	Common-mode	V_{CM} = (V–) –0.1 V to (V+) –3.5 V			10^{13} || 7		Ω || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	V_O = (V–) + 0.35 V to (V+) – 0.35 V, R_L = 10 kΩ		120	126		dB
		V_O = (V–) + 0.35 V to (V+) – 0.35 V, R_L = 2 kΩ		114	126		
			T_A = –40°C to +125°C	108			
FREQUENCY RESPONSE							
BW	Gain bandwidth product				11		MHz
SR	Slew rate				20		V/µs
t_s	Settling time	12 bits			0.88		µs
		16 bits			1.6		
t_{OR}	Overload recovery time				600		ns
THD+N	Total harmonic distortion + noise	1 kHz, G = +1, V_O = 3.5 V_{RMS}			0.00005%		
OUTPUT							
V_O	Voltage output	R_L = 10 kΩ, A_{OL} ≥ 108 dB		(V–) + 0.2		(V+) – 0.2	V
		R_L = 2 kΩ, A_{OL} ≥ 108 dB		(V–) + 0.35		(V+) – 0.35	
I_{SC}	Short-circuit current	Source			36		mA
		Sink			–30		
C_{LOAD}	Capacitive load drive				See *Typical Characteristics*		
Z_O	Open-loop output impedance	f = 1 MHz, I_O = 0 A (See *Typical Characteristics*)			16		Ω

6.7 Electrical Characteristics （续）

at T_A = 25°C, V_S = 4.5 V (±2.25) to 36 V (±18 V), R_L = 2 kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
I_Q	Quiescent current per amplifier	I_O = 0 mA		1.8	2	mA
		T_A = –40°C to +125°C			2.7	
CHANNEL SEPARATION						
	Channel separation	At dc		0.02		µV/V
		At 100 kHz		10		

6.8 Typical Characteristics

at T_A = 25°C, V_S = ±18 V, R_L = 2 kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

表 6-1. Table of Graphs

DESCRIPTION	FIGURE
Offset Voltage Production Distribution	图 6-1
Offset Voltage Drift Distribution	图 6-2
Offset Voltage vs Common-Mode Voltage (Maximum Supply)	图 6-3
Input Offset Voltage vs Temperature	图 6-4
I_B vs Common-Mode Voltage	图 6-5
Output Voltage Swing vs Output Current	图 6-6
CMRR and PSRR vs Frequency (RTI)	图 6-7
Common-Mode Rejection Ratio vs Temperature	图 6-8
0.1-Hz to 10-Hz Noise	图 6-9
Input Voltage Noise Density vs Frequency	图 6-10
THD+N Ratio vs Frequency (80-kHz AP Bandwidth)	图 6-11
THD+N Ratio vs Output Amplitude	图 6-12
Quiescent Current vs Temperature	图 6-13
Quiescent Current vs Supply Voltage	图 6-14
Gain and Phase vs Frequency	图 6-15
Closed-Loop Gain vs Frequency	图 6-16
Open-Loop Gain vs Temperature	图 6-17
Open-Loop Output Impedance vs Frequency	图 6-18
Small-Signal Overshoot vs Capacitive Load (G = 1)	图 6-19
Small-Signal Overshoot vs Capacitive Load (G = –1)	图 6-20
No Phase Reversal	图 6-21
Maximum Output Voltage vs Frequency	图 6-22
Positive Overload Recovery	图 6-23
Negative Overload Recovery	图 6-24
Large-Signal Positive and Negative Settling Time	图 6-25, 图 6-26
Small-Signal Step Response (G = 1)	图 6-27
Small-Signal Step Response (G = –1)	图 6-28
Large-Signal Step Response (G = 1)	图 6-29
Large-Signal Step Response (G = –1)	图 6-30
Short-Circuit Current vs Temperature	图 6-31

6.8 Typical Characteristics

at T_A = 25°C, V_S = ±18 V, R_L = 2 kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

表 6-1. Table of Graphs （续）

DESCRIPTION	FIGURE
Channel Separation vs Frequency	图 6-32

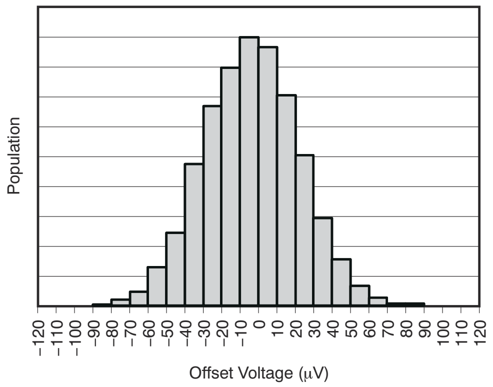


图 6-1. Offset Voltage Production Distribution

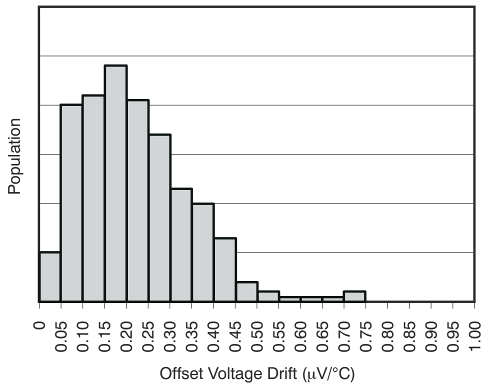


图 6-2. Offset Voltage Drift Distribution

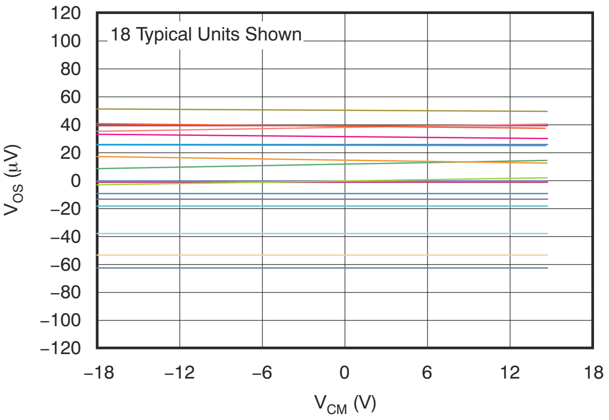


图 6-3. Offset Voltage vs Common-Mode Voltage

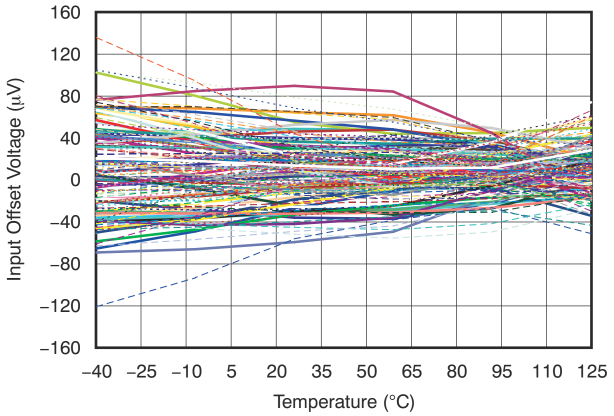


图 6-4. Input Offset Voltage vs Temperature (144 Amplifiers)

6.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, R_L = 2 kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

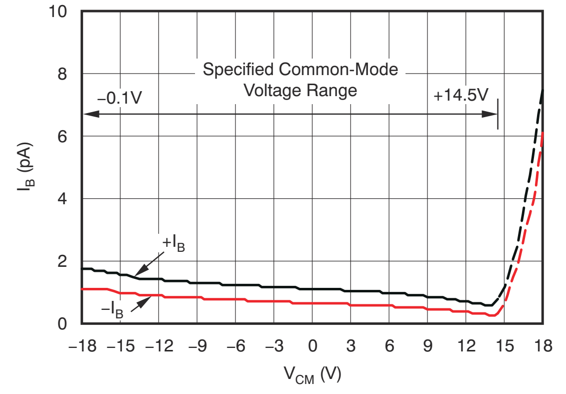


图 6-5. I_B vs Common-Mode Voltage

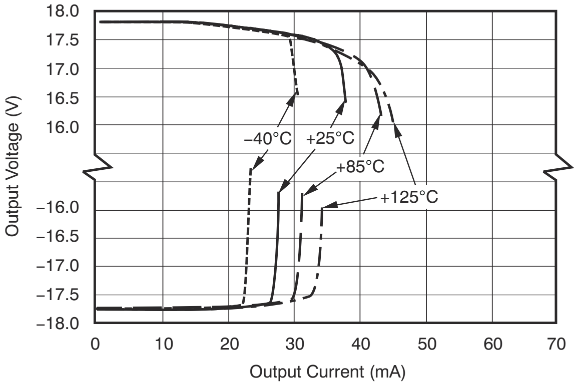


图 6-6. Output Voltage Swing vs Output Current (Maximum Supply)

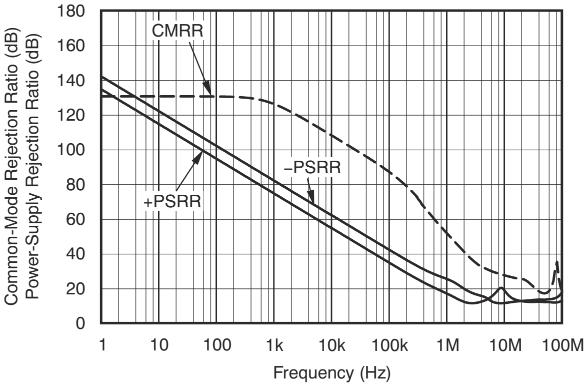


图 6-7. CMRR and PSRR vs Frequency (Referred to Input)

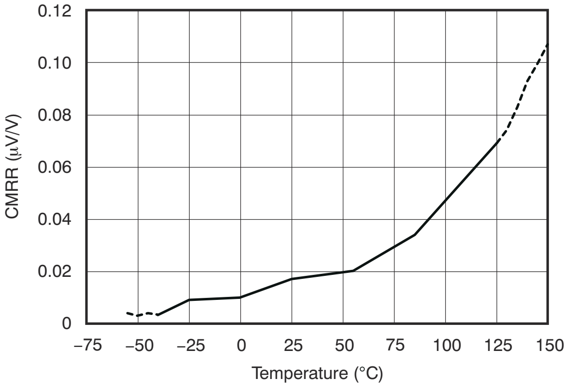


图 6-8. Common-Mode Rejection Ratio vs Temperature

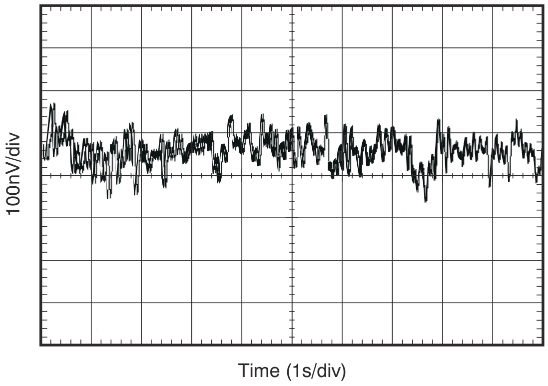


图 6-9. 0.1-Hz to 10-Hz Noise

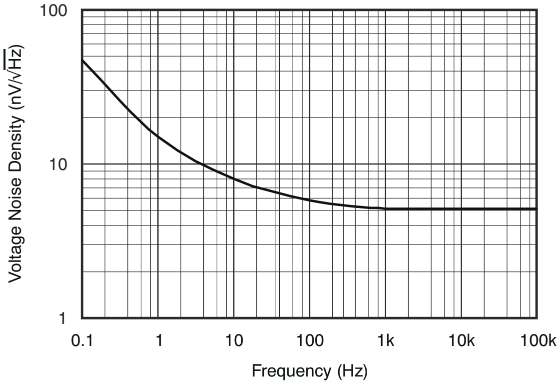


图 6-10. Input Voltage Noise Density vs Frequency

6.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, R_L = 2 kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

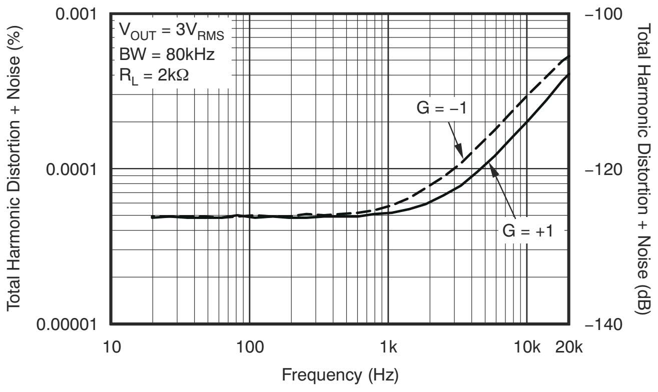


图 6-11. THD+N Ratio vs Frequency

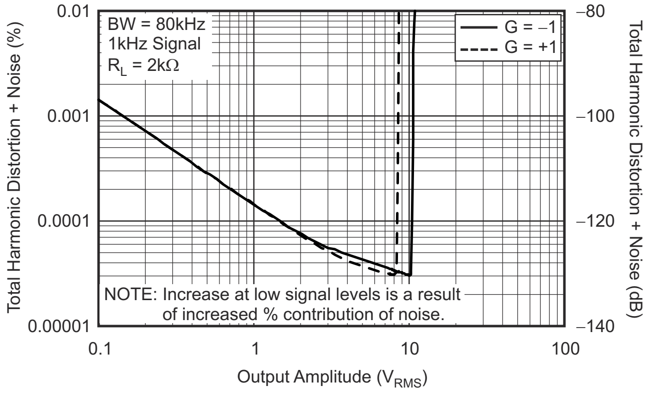


图 6-12. THD+N Ratio vs Output Amplitude

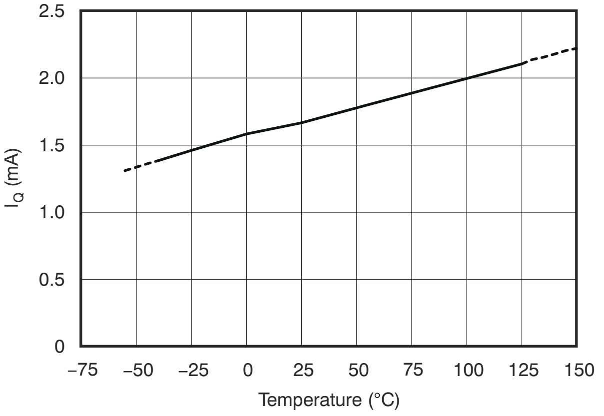


图 6-13. Quiescent Current vs Temperature

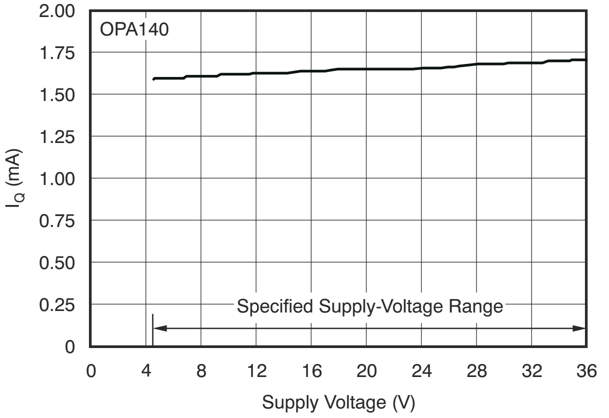


图 6-14. Quiescent Current vs Supply Voltage

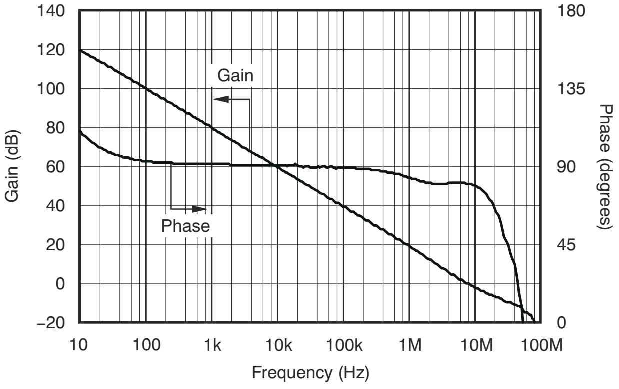


图 6-15. Gain and Phase vs Frequency

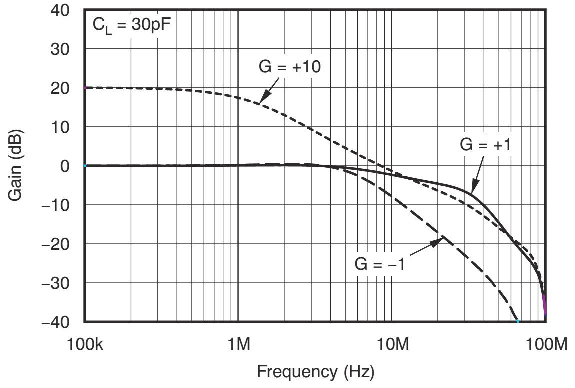


图 6-16. Closed-Loop Gain vs Frequency

6.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, R_L = 2 kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

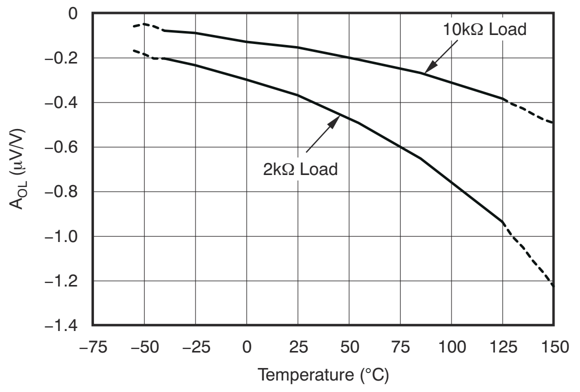


图 6-17. Open-Loop Gain vs Temperature

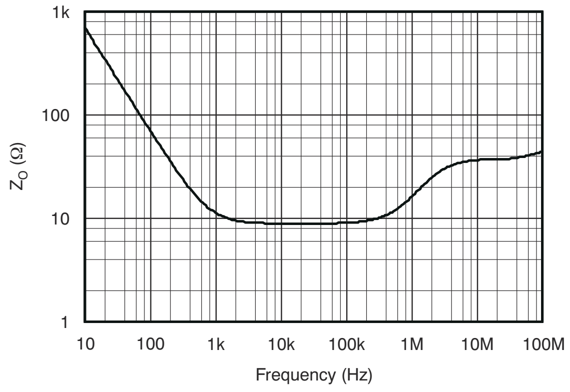


图 6-18. Open-Loop Output Impedance vs Frequency

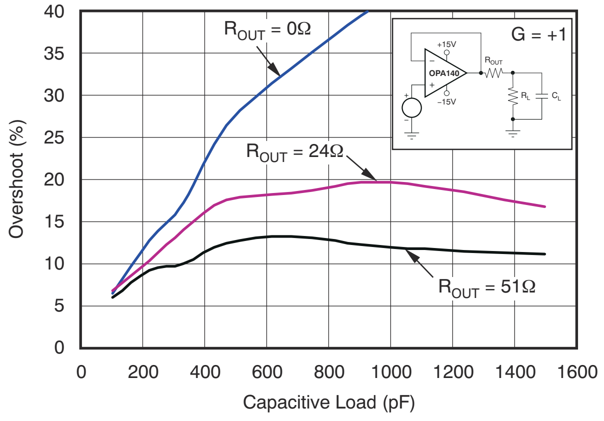


图 6-19. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

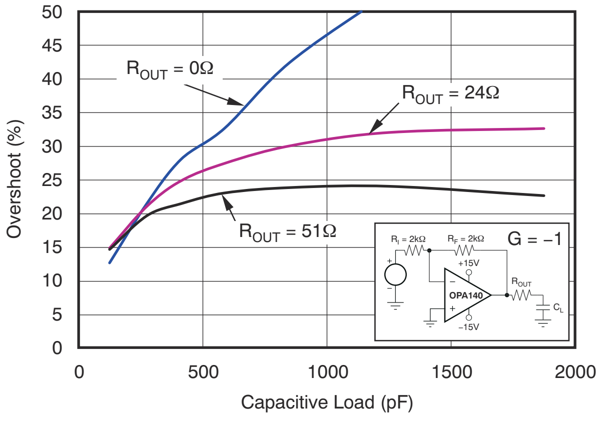


图 6-20. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

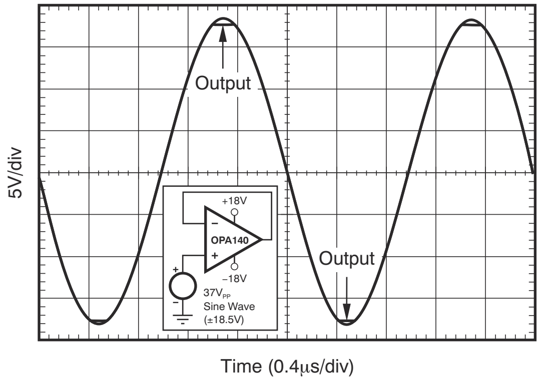


图 6-21. No Phase Reversal

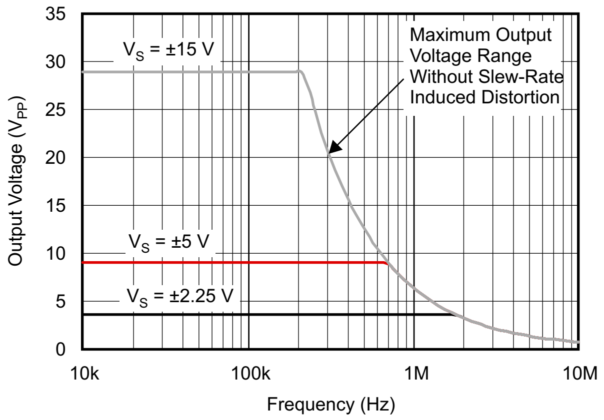


图 6-22. Maximum Output Voltage vs Frequency

6.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, R_L = 2 kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

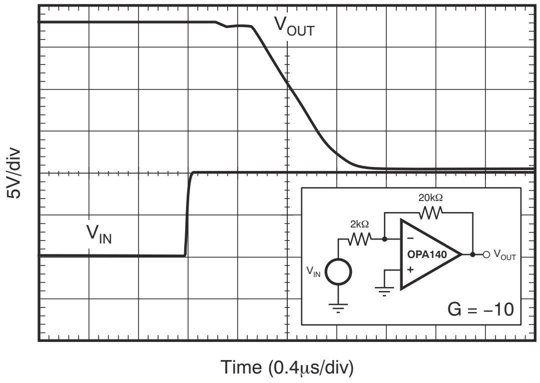


图 6-23. Positive Overload Recovery

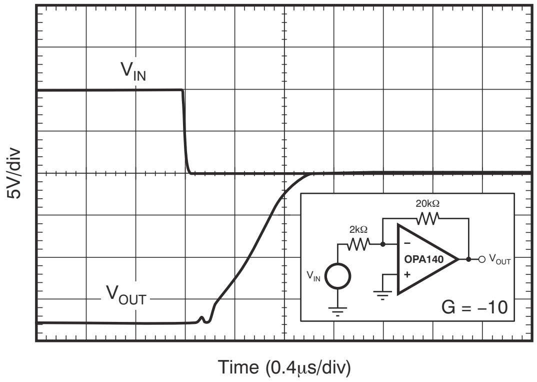


图 6-24. Negative Overload Recovery

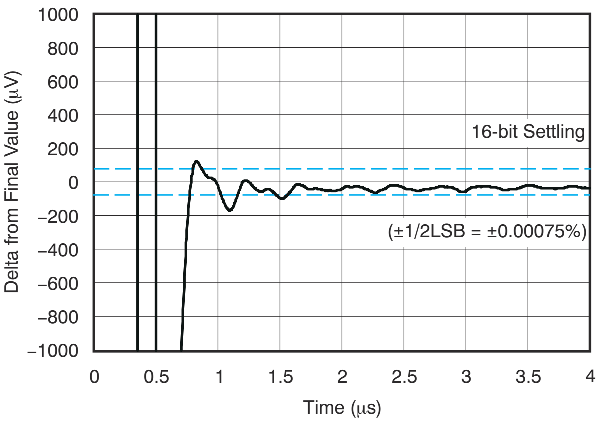


图 6-25. Large-Signal Positive Settling Time (10-V Step)

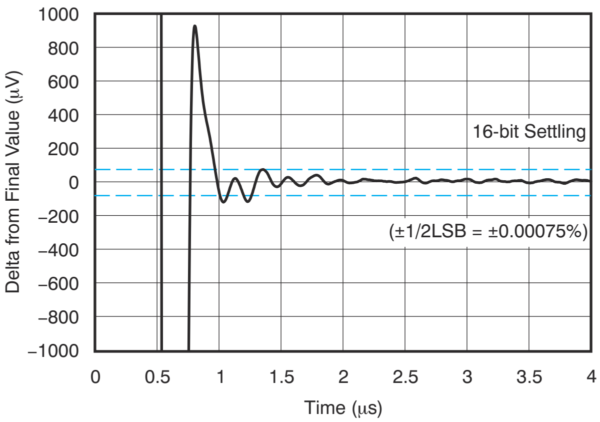


图 6-26. Large-Signal Negative Settling Time (10-V Step)

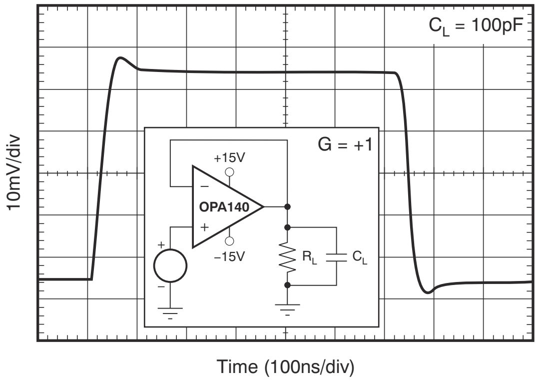


图 6-27. Small-Signal Step Response (100 mV)

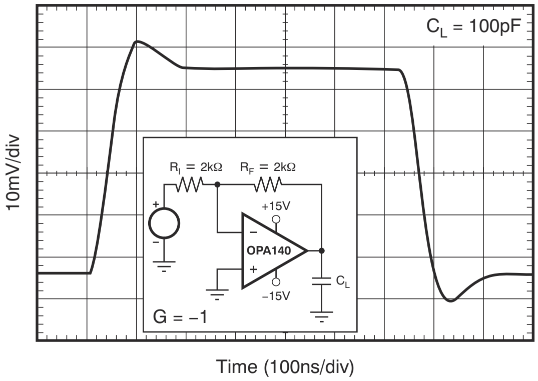


图 6-28. Small-Signal Step Response (100 mV)

6.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, R_L = 2 kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

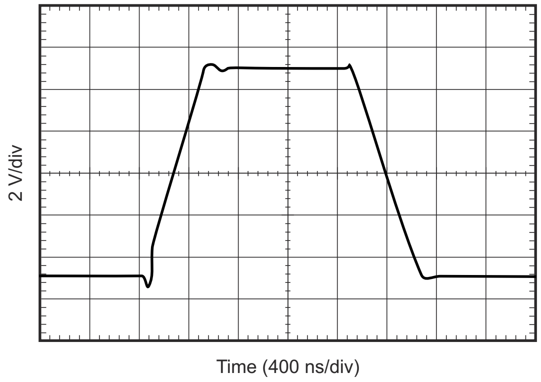


图 6-29. Large-Signal Step Response

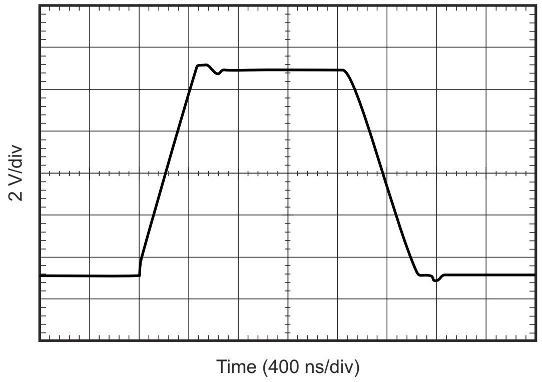


图 6-30. Large-Signal Step Response

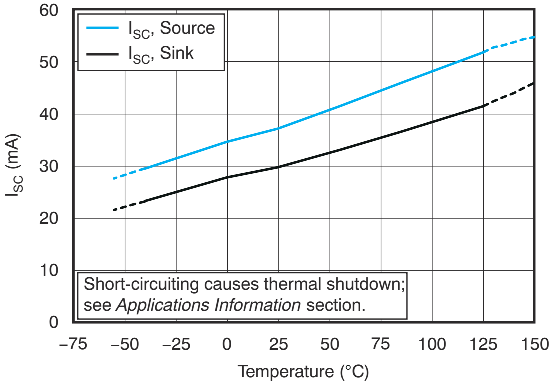


图 6-31. Short Circuit Current vs Temperature

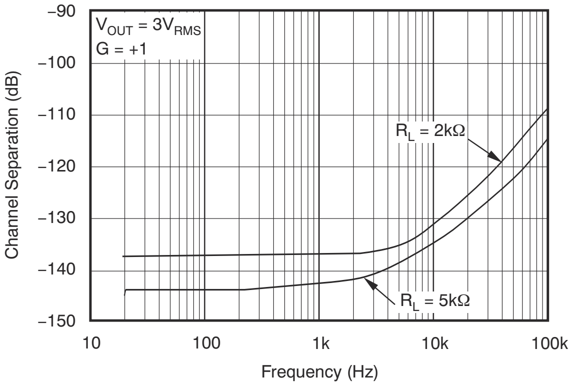


图 6-32. Channel Separation vs Frequency

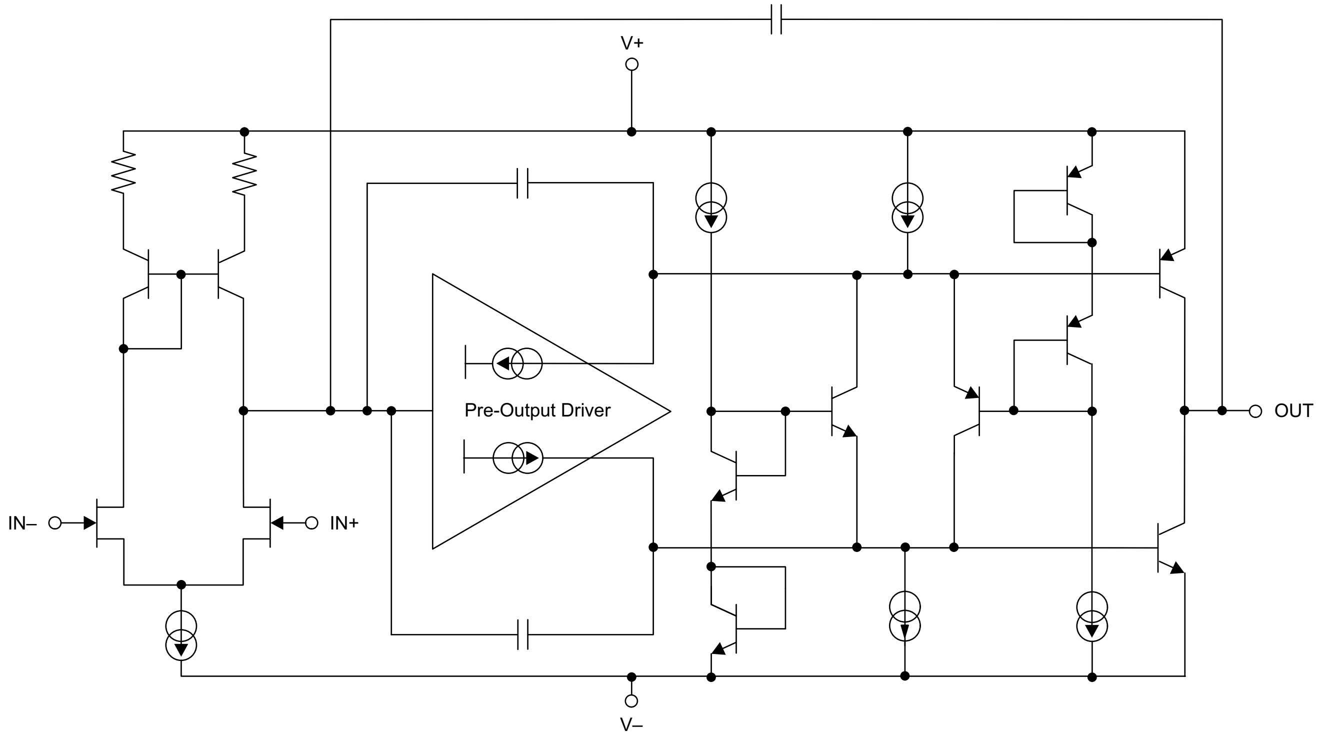
7 Detailed Description

7.1 Overview

The OPAx140 family of operational amplifiers is a series of low-power JFET input amplifiers that feature excellent drift performance and low input bias current. The rail-to-rail output swing and input range that includes V– allow designers to use the low-noise characteristics of JFET amplifiers while also interfacing to modern, single-supply, precision analog-to-digital converters (ADCs) and digital-to-analog converters (DACs). The OPAx140 series achieves 11-MHz unity-gain bandwidth and 20-V/μs slew rate, and consumes only 1.8 mA (typical) of quiescent current. These devices operate on a single 4.5-V to 36-V supply or dual ±2.25-V to ±18-V supplies.

节 7.2 shows the simplified diagram of the OPAx140.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Operating Voltage

The OPA140, OPA2140, and OPA4140 series of op amps can be used with single or dual supplies from an operating range of V_S = 4.5 V (±2.25 V) and up to V_S = 36 V (±18 V). These devices do not require symmetrical supplies, but only a minimum supply voltage of 4.5 V (±2.25 V). For V_S less than ±3.5 V, the common-mode input range does not include midsupply. Supply voltages higher than 40 V can permanently damage the device; see *节 6.1*. Key parameters are specified over the operating temperature range, T_A = –40°C to 125°C. Key parameters that vary over the supply voltage or temperature range are shown in *节 6.8* of this data sheet.

7.3.2 Capacitive Load and Stability

The dynamic characteristics of the OPAx140 have been optimized for commonly encountered gains, loads, and operating conditions. The combination of low closed-loop gain and high capacitive loads decreases the phase margin of the amplifier and can lead to gain peaking or oscillations. As a result, heavier capacitive loads must be isolated from the output. The simplest way to achieve this isolation is to add a small resistor (R_{OUT} equal to 50 Ω, for example) in series with the output.

图 6-19 and 图 6-20 illustrate graphs of *Small-Signal Overshoot vs Capacitive Load* for several values of R_{OUT}. Also, see the *Feedback Plots Define Op Amp AC Performance Application Bulletin*, available for download from www.ti.com, for details of analysis techniques and application circuits.

7.3.3 Output Current Limit

The output current of the OPAx140 series is limited by internal circuitry to 36 mA/–30 mA (sourcing/sinking), to protect the device if the output is accidentally shorted. This short circuit current depends on temperature, as shown in 图 6-31.

7.3.4 Noise Performance

图 7-1 shows the total circuit noise for varying source impedances with the operational amplifier in a unity-gain configuration (with no feedback resistor network and therefore no additional noise contributions). The OPA140 and OPA211 are shown with total circuit noise calculated. The op amp contributes both a voltage noise component and a current noise component. The voltage noise is commonly modeled as a time-varying component of the offset voltage. The current noise is modeled as the time-varying component of the input bias current and reacts with the source resistance to create a voltage component of noise. Therefore, the lowest noise op amp for a given application depends on the source impedance. For low source impedance, current noise is negligible, and voltage noise generally dominates. The OPAx140 family has both low voltage noise and extremely low current noise because of the FET input of the op amp. As a result, the current noise contribution of the OPAx140 series is negligible for any practical source impedance, which makes these devices the better choice for applications with high source impedance.

The equation in 图 7-1 shows the calculation of the total circuit noise, with these parameters:

- e_n = voltage noise
- I_n = current noise
- R_S = source impedance
- k = Boltzmann's constant = 1.38×10^{-23} J/K
- T = temperature in kelvins (K)

For more details on calculating noise, see *节 7.3.5*.

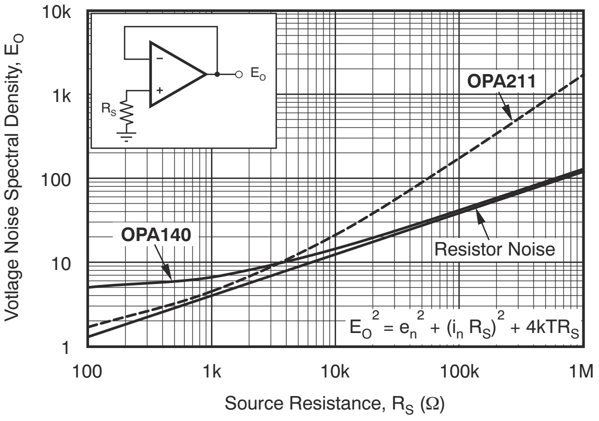


图 7-1. Noise Performance of the OPA140 and OPA211 in Unity-Gain Buffer Configuration

7.3.5 Basic Noise Calculations

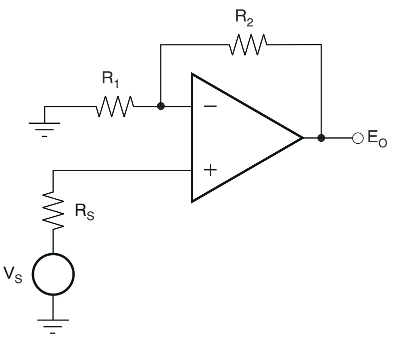
Low-noise circuit design requires careful analysis of all noise sources. External noise sources can dominate in many cases; consider the effect of source resistance on overall op amp noise performance. Total noise of the circuit is the root-sum-square combination of all noise components.

The resistive portion of the source impedance produces thermal noise proportional to the square root of the resistance. This function is plotted in 图 7-1. The source impedance is usually fixed; consequently, select the op amp and the feedback resistors to minimize the respective contributions to the total noise.

图 7-2 illustrates both noninverting **(A)** and inverting **(B)** op amp circuit configurations with gain. In circuit configurations with gain, the feedback network resistors also contribute noise. In general, the current noise of the op amp reacts with the feedback resistors to create additional noise components. However, the extremely low current noise of the OPAx140 means that the current noise contribution can be neglected.

The feedback resistor values can generally be chosen to make these noise sources negligible. Low impedance feedback resistors load the output of the amplifier. The equations for total noise are shown for both configurations.

A) Noise in Noninverting Gain Configuration



Noise at the output:

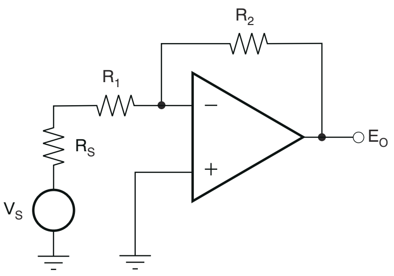
$$E_O^2 = \left(1 + \frac{R_2}{R_1}\right)^2 e_n^2 + \left(\frac{R_2}{R_1}\right)^2 e_1^2 + e_2^2 + \left(1 + \frac{R_2}{R_1}\right)^2 e_s^2$$

Where $e_S = \sqrt{4kTR_S}$ = thermal noise of R_S

$e_1 = \sqrt{4kTR_1}$ = thermal noise of R_1

$e_2 = \sqrt{4kTR_2}$ = thermal noise of R_2

B) Noise in Inverting Gain Configuration



Noise at the output:

$$E_O^2 = \left(1 + \frac{R_2}{R_1 + R_S}\right)^2 e_n^2 + \left(\frac{R_2}{R_1 + R_S}\right)^2 e_1^2 + e_2^2 + \left(\frac{R_2}{R_1 + R_S}\right)^2 e_s^2$$

Where $e_S = \sqrt{4kTR_S}$ = thermal noise of R_S

$e_1 = \sqrt{4kTR_1}$ = thermal noise of R_1

$e_2 = \sqrt{4kTR_2}$ = thermal noise of R_2

For the OPAx140 series of operational amplifiers at 1 kHz, $e_n = 5.1\ \text{nV}/\sqrt{\text{Hz}}$.

图 7-2. Noise Calculation in Gain Configurations

7.3.6 Phase-Reversal Protection

The OPA140, OPA2140, and OPA4140 family has internal phase-reversal protection. Many FET- and bipolar-input op amps exhibit a phase reversal when the input is driven beyond the linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The input circuitry of the OPA140, OPA2140, and OPA4140 prevents phase reversal with excessive common-mode voltage; instead, the output limits into the appropriate rail (see 图 6-21).

7.3.7 Thermal Protection

The OPAx140 series of op amps are capable of driving 2-kΩ loads with power-supply voltages of up to ±18 V over the specified temperature range. In a single-supply configuration, where the load is connected to the negative supply voltage, the minimum load resistance is 2.8 kΩ at a supply voltage of 36 V. For lower supply voltages (either single-supply or symmetrical supplies), a lower load resistance can be used, as long as the output current does not exceed 13 mA; otherwise, the device short circuit current protection circuit can activate.

Internal power dissipation increases when operating at high supply voltages. Copper leadframe construction used in the OPA140, OPA2140, and OPA4140 series devices improves heat dissipation compared to conventional materials. Printed-circuit-board (PCB) layout can also help reduce a possible increase in junction temperature (T_J). Wide copper traces help dissipate the heat by acting as an additional heatsink. Temperature rise can be further minimized by soldering the devices directly to the PCB rather than using a socket.

Although the output current is limited by internal protection circuitry, accidental shorting of one or more output channels of a device can result in excessive heating. For instance, when an output is shorted to mid-supply, the typical short-circuit current of 36 mA leads to an internal power dissipation of over 600 mW at a supply of ±18 V. Total power dissipation (P_D) includes both the quiescent power dissipation (P_{DQ}) and the power dissipation due to the load (P_{DL}).

In the case of a dual OPA2140 in an 8-pin VSSOP package (the junction-to-ambient thermal resistance, $R_{\theta JA}$, is 180°C/W), such power dissipation can lead the die temperature to be 220°C above ambient temperature (T_A), when both channels are shorted. This temperature increase significantly decreases the operating life of the device. T_J can be approximated using 方程式 1.

$$T_J = T_A + (P_{DQ} + P_{DL}) \times R_{\theta JA} \tag{1}$$

To prevent excessive heating, the OPAx140 series has an internal thermal shutdown circuit that shuts down the device if the die temperature exceeds approximately 180°C. When this thermal shutdown circuit activates, a built-in hysteresis of 15°C makes sure that the die temperature must drop to approximately 165°C before the device switches on again.

Additional consideration is needed for the combination of maximum operating voltage, maximum operating temperature, load, and package type. 图 7-3 and 图 7-4 show several practical considerations when evaluating the OPA2140 (dual version) and the OPA4140 (quad version).

As an example, the OPA4140 has a maximum total quiescent current of 10.8 mA (2.7 mA/channel) over temperature. The 14-pin TSSOP package has a typical $R_{\theta JA}$ of 135°C/W. This parameter means that because T_J must not exceed 150°C to provide reliable operation, either the supply voltage must be reduced, or T_A needs to remain low enough so that the T_J does not exceed 150°C. This condition is illustrated in 图 7-3 for various package types.

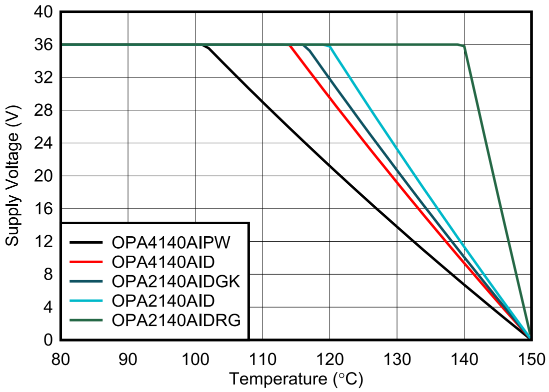


图 7-3. Maximum Supply Voltage vs Temperature, Quiescent State (No Load)

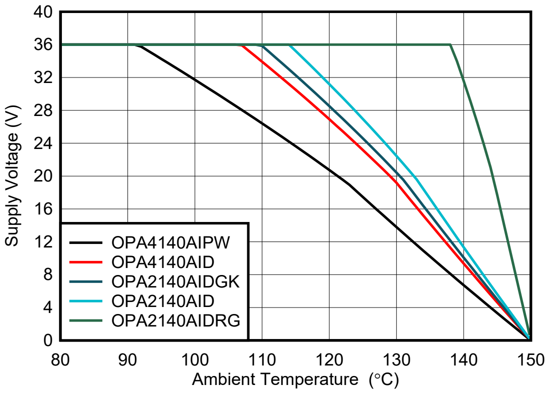


图 7-4. Maximum Supply Voltage vs Temperature, DC Worst-Case

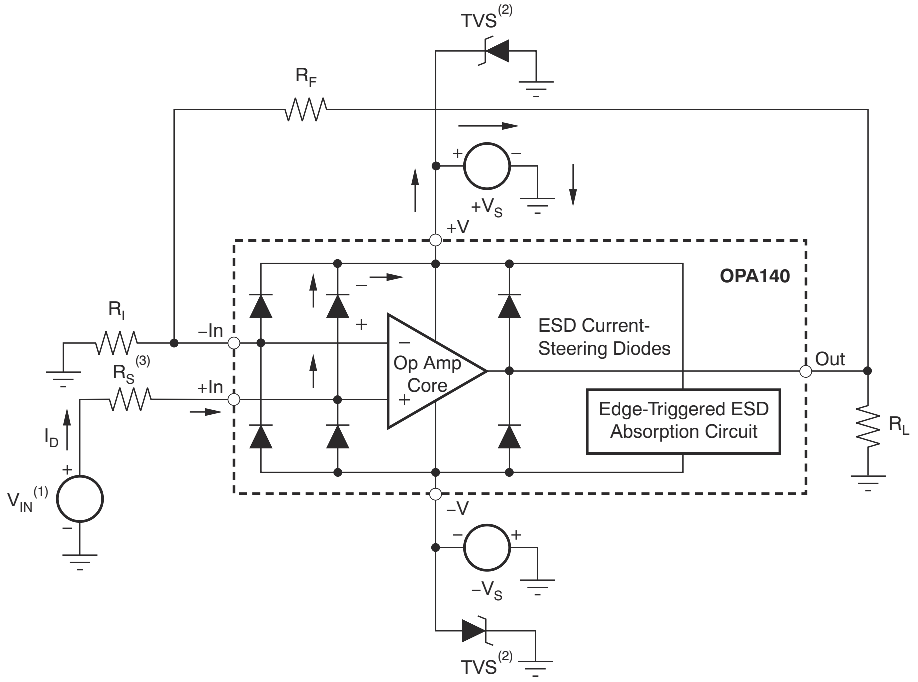
Moreover, resistive loading of the output causes additional power dissipation and thus self-heating, which also must be considered when establishing the maximum supply voltage or operating temperature. To this end, 图 7-4 shows the maximum supply voltage versus temperature for a 2 kΩ load resistance to mid-supply and a dc worst-case power dissipation condition. In symmetrical, bipolar supplies, the worst case dc condition is given by $V_{OUT} = \pm V_S/4$.

As shown by 方程式 1, the junction temperature depends on the thermal properties of the package, as expressed by $R_{\Theta JA}$. If the device then begins to drive a heavy load, the junction temperature can rise and trip the thermal-shutdown circuit. For such loading cases, the DRG package includes a thermal pad that significantly reduces $R_{\Theta JA}$. Proper PCB layout is essential to realize this improved thermal behavior. 图 7-3 and 图 7-3 show the potential improvement when using the DRG package option. For more information on PCB layout best practices, see 节 8.4.1.

7.3.8 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but can involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

A good understanding of this basic ESD circuitry and the relevance to an electrical overstress event is helpful. 图 7-5 shows an illustration of the ESD circuits contained in the OPAx140 series (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.



(1) $V_{IN} = +V_S + 500$ mV.
(2) TVS: $+V_{S(max)} > V_{TVSBR\ (Min)} > +V_S$
(3) Suggested value approximately 1 kΩ.

图 7-5. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application

An ESD event produces a short duration, high-voltage pulse that is transformed into a short duration, high-current pulse when discharging through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent damage. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more of the amplifier device pins, current flows through one or more of the steering diodes. Depending on the path that the current takes, the absorption device can activate. The absorption device has a trigger, or threshold voltage, that is above the normal operating voltage of the OPAx140 but below the device breakdown voltage level. When this threshold is exceeded, the absorption device quickly activates and clamps the voltage across the supply rails to a safe level.

When the operational amplifier connects into a circuit, as 图 7-5 shows, the ESD protection components are intended to remain inactive and not become involved in the application circuit operation. However, circumstances can arise where an applied voltage exceeds the operating voltage range of a given pin. If this condition occurs, there is a risk that some of the internal ESD protection circuits can be biased on and conduct current. Any such current flow occurs through steering diode paths and rarely involves the absorption device.

图 7-5 shows a specific example where the input voltage, V_{IN}, exceeds the positive supply voltage ($+V_S$) by 500 mV or more. Much of what happens in the circuit depends on the supply characteristics. If $+V_S$ can sink the current, one of the upper input steering diodes conducts and directs current to $+V_S$. Excessively high current levels can flow with increasingly higher V_{IN}. As a result, the data sheet specifications recommend that applications limit the input current to 10 mA.

If the supply is not capable of sinking the current, V_{IN} can begin sourcing current to the operational amplifier, and then take over as the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the operational amplifier absolute maximum ratings.

Another common question involves what happens to the amplifier if an input signal is applied to the input while the power supplies $+V_S$ or $–V_S$ are at 0 V. Again, the answer depends on the supply characteristic while at 0 V, or at a level below the input signal amplitude. If the supplies appear as high impedance, then the operational amplifier supply current can be supplied by the input source through the current steering diodes. This state is not a normal bias condition; the amplifier most likely does not operate normally. If the supplies are low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current, and any resistance in the input path.

If there is an uncertainty about the ability of the supply to absorb this current, external Zener diodes can be added to the supply pins; see 图 7-5. Select the Zener voltage so that the diode does not turn on during normal operation. However, the Zener voltage must be low enough so that the Zener diode conducts if the supply pin begins to exceed the safe operating supply voltage level.

7.3.9 EMI Rejection

The electromagnetic interference (EMI) rejection ratio, or EMIRR, describes the EMI immunity of operational amplifiers. An adverse effect that is common to many op amps is a change in the offset voltage as a result of RF signal rectification. An op amp that is more efficient at rejecting this change in offset as a result of EMI has a higher EMIRR and is quantified by a decibel value. Measuring EMIRR can be performed in many ways, but this section provides the EMIRR IN+, which specifically describes the EMIRR performance when the RF signal is applied to the noninverting input pin of the op amp. In general, only the noninverting input is tested for EMIRR for the following three reasons:

- Op amp input pins are known to be the most sensitive to EMI, and typically rectify RF signals better than the supply or output pins.
- The noninverting and inverting op amp inputs have symmetrical physical layouts and exhibit nearly matching EMIRR performance
- EMIRR is easier to measure on noninverting pins than on other pins because the noninverting input terminal can be isolated on a PCB. This isolation allows the RF signal to be applied directly to the noninverting input terminal with no complex interactions from other components or connecting PCB traces. 图 7-6

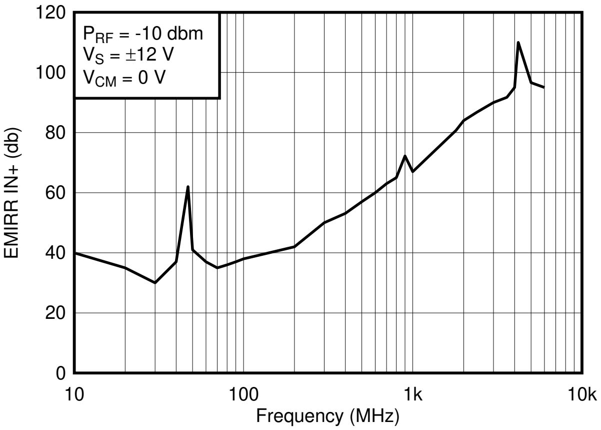


图 7-6. OPA2140 EMIRR

The EMIRR IN+ of the OPA2140 is plotted versus frequency as shown in .If available, any dual and quad op amp device versions have nearly similar EMIRR IN+ performance. The OPA2140 unity-gain bandwidth is 11 MHz. EMIRR performance below this frequency denotes interfering signals that fall within the op amp bandwidth.

For more information, see the *EMI Rejection Ratio of Operational Amplifiers Application Report*, available for download from www.ti.com.

表 7-1 lists the EMIRR IN+ values for the OPA2140 at particular frequencies commonly encountered in real-world applications. Applications listed in 表 7-1 can be centered on or operated near the particular frequency shown. This information can be of special interest to designers working with these types of applications, or working in other fields likely to encounter RF interference from broad sources, such as the industrial, scientific, and medical (ISM) radio band.

表 7-1. OPA2140 EMIRR IN+ for Frequencies of Interest

FREQUENCY	APPLICATION OR ALLOCATION	EMIRR IN+
400 MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultra-high frequency (UHF) applications	53.1 dB
900 MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6 GHz), GSM, aeronautical mobile, UHF applications	72.2 dB
1.8 GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1 GHz to 2 GHz)	80.7 dB
2.4 GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2 GHz to 4 GHz)	86.8 dB
3.6 GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	91.7 dB
5 GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4 GHz to 8 GHz)	96.6 dB

7.3.10 EMIRR +IN Test Configuration

图 7-7 shows the circuit configuration for testing the EMIRR IN+. An RF source is connected to the op amp noninverting input terminal using a transmission line. The op amp is configured in a unity gain buffer topology with the output connected to a low-pass filter (LPF) and a digital multimeter (DMM). A large impedance mismatch at the op amp input causes a voltage reflection; however, this effect is characterized and accounted for when determining the EMIRR IN+. The resulting DC offset voltage is sampled and measured by the multimeter. The LPF isolates the multimeter from residual RF signals that can interfere with multimeter accuracy.

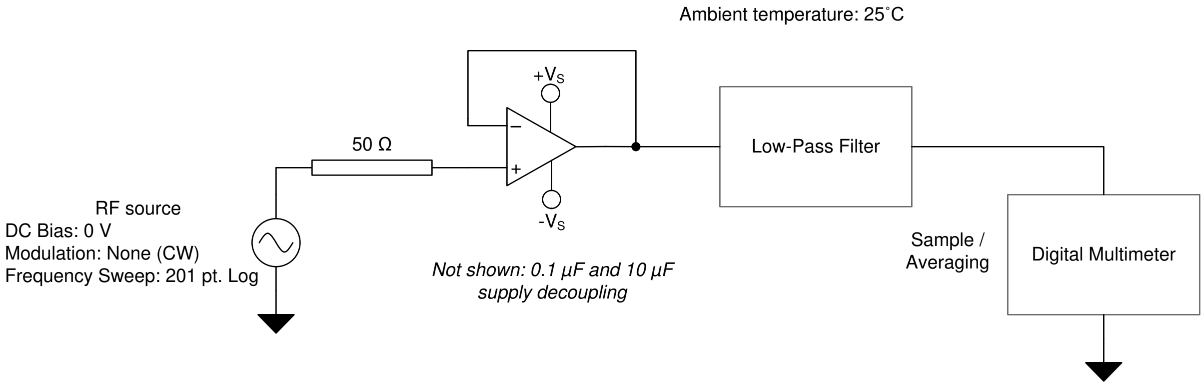


图 7-7. EMIRR +IN Test Configuration

7.4 Device Functional Modes

The OPAx140 has a single functional mode and is operational when the power-supply voltage is greater than 4.5 V (±2.25 V). The maximum power supply voltage for the OPAx140 is 36 V (±18 V).

8 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

The OPA140, OPA2140, and OPA4140 are unity-gain stable, operational amplifiers with very low noise, input bias current, and input offset voltage. Applications with noisy or high-impedance power supplies require decoupling capacitors placed close to the device pins. In most cases, 0.1-µF capacitors are adequate. Designers can easily use the rail-to-rail output swing and input range that includes V– to take advantage of the low-noise characteristics of JFET amplifiers while also interfacing to modern, single-supply, precision data converters.

8.2 Typical Application

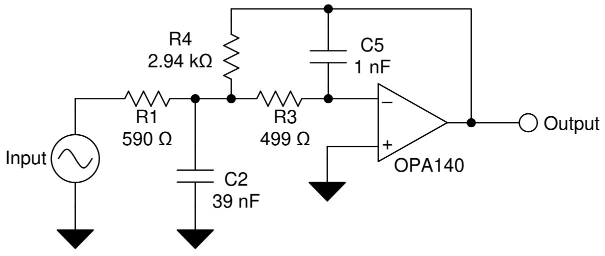


图 8-1. 25-kHz Low-pass Filter

8.2.1 Design Requirements

Low-pass filters are commonly employed in signal processing applications to reduce noise and prevent aliasing. The OPAx140 are an excellent choice to construct high-speed, high-precision active filters. 图 8-1 shows a second-order, low-pass filter commonly encountered in signal processing applications.

Use the following parameters for this design example:

- Gain = 5 V/V (inverting gain)
- Low-pass cutoff frequency = 25 kHz
- Second-order Chebyshev filter response with 3-dB gain peaking in the pass band

8.2.2 Detailed Design Procedure

The infinite-gain multiple-feedback circuit for a low-pass network function is shown in. Use 方程式 2 to calculate the voltage transfer function.

$$\frac{\text{Output}}{\text{Input}}(s) = \frac{-1/R_1R_3C_2C_5}{s^2 + (s/C_2)(1/R_1 + 1/R_3 + 1/R_4) + 1/R_3R_4C_2C_5} \tag{2}$$

This circuit produces a signal inversion. For this circuit, the gain at DC and the low-pass cutoff frequency are calculated by 方程式 3:

$$\text{Gain} = \frac{R_4}{R_1}$$

$$f_C = \frac{1}{2\pi}\sqrt{(1/R_3R_4C_2C_5)} \tag{3}$$

Software tools are readily available to simplify filter design. The WEBENCH® Filter Designer is a simple, powerful, and easy-to-use active filter design program. The WEBENCH® Filter Designer lets you create optimized filter designs using a selection of TI operational amplifiers and passive components from TI's vendor partners.

Available as a web based tool from the WEBENCH Design Center, the WEBENCH Filter Designer allows you to design, optimize, and simulate complete, multistage, active-filter solutions within minutes.

8.2.3 Application Curve

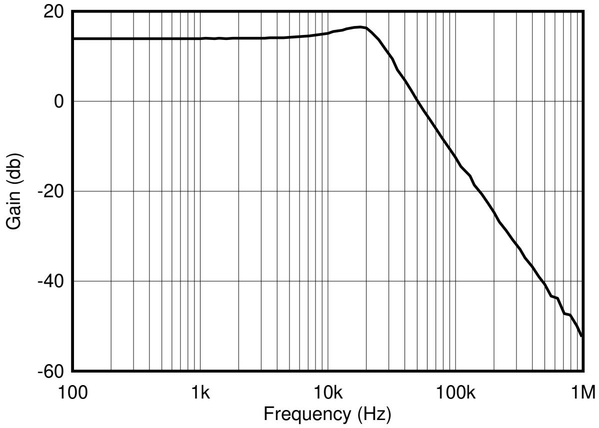


图 8-2. OPAx140 Second-Order, 25-kHz, Chebyshev, Low-Pass Filter

8.3 Power Supply Recommendations

The OPAx140 is specified for operation from 4.5 V to 36 V (±2.25 V to ±18 V); many specifications apply from –40°C to 125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in *节 6.8*.

小心

Supply voltages larger than 40 V can permanently damage the device; see *节 6.1*.

Place 0.1-μF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see *节 8.4*.

8.4 Layout

8.4.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

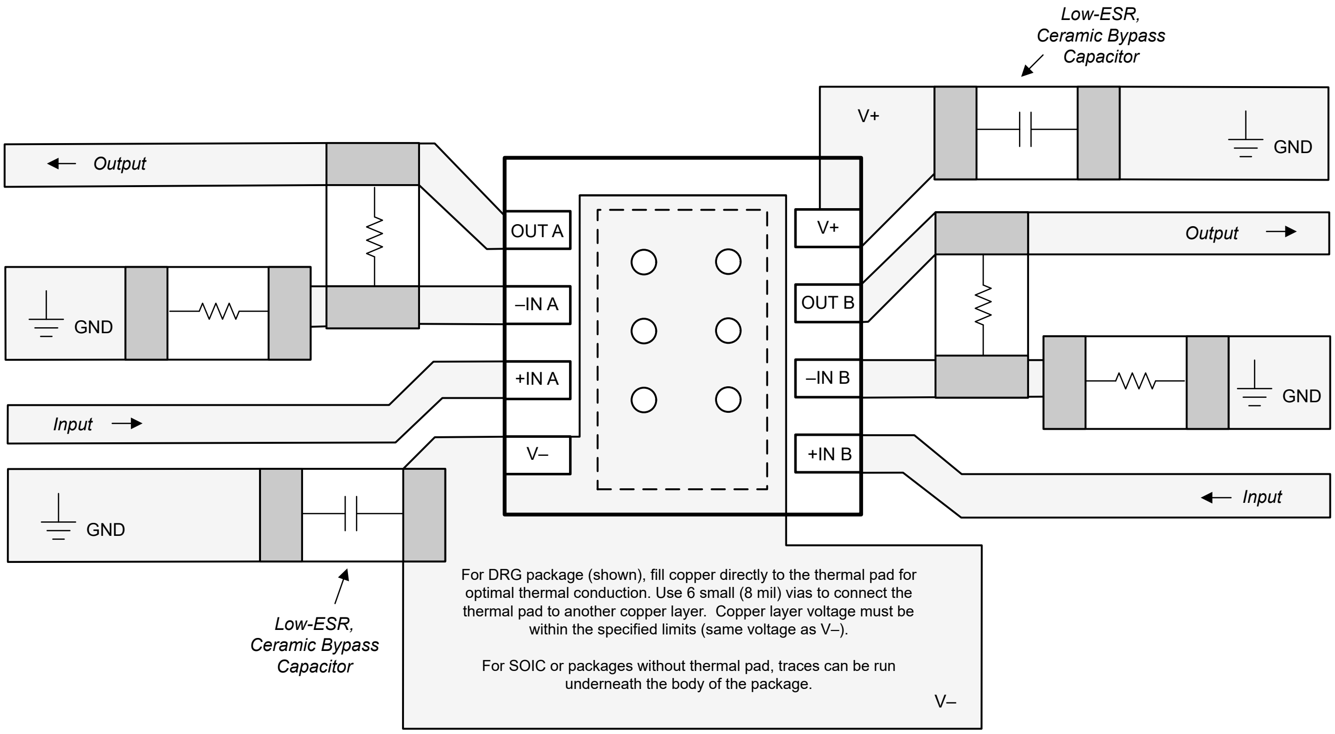
- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-μF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current. For more detailed information, see *Circuit Board Layout Techniques*.

- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As illustrated in 图 8-3, keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- For best performance, TI recommends cleaning the PCB following board assembly.
- Any precision integrated circuit can experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, TI recommends baking the PCB assembly to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

In addition, follow these steps for the DRG package:

- Solder the thermal pad to a V− plane to conduct heat away from the package. Thermal vias underneath the thermal pad are recommended, but not required. The recommended pattern is shown in the mechanical drawing appended to the end of this document. If using thermal vias connect to the V− plane.
- When connecting these vias to the plane, do not use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations, making the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the vias under the package must make the connections to the internal plane with a complete connection around the entire circumference of the plated-through hole.
- The top-side solder mask must leave the pins of the package and the thermal pad area exposed. The bottom-side solder mask must cover the vias of the thermal pad area. This masking prevents solder from being pulled away from the thermal pad area during the reflow process.
- Apply solder paste to the exposed thermal pad area and all of the device pins.
- With these preparatory steps in place, simply place the device in position, and run through the solder reflow operation as with any standard surface-mount component

8.4.2 Layout Example



For DRG package (shown), fill copper directly to the thermal pad for optimal thermal conduction. Use 6 small (8 mil) vias to connect the thermal pad to another copper layer. Copper layer voltage must be within the specified limits (same voltage as V–).

For SOIC or packages without thermal pad, traces can be run underneath the body of the package.

图 8-3. Dual Operational Amplifier Board Layout for Noninverting Configuration

9 Device and Documentation Support

9.1 Device Support

9.1.1 Development Support

9.1.1.1 PSpice® for TI

PSpice® for TI 是可帮助评估模拟电路性能的设计和仿真环境。在进行布局和制造之前创建子系统设计和原型解决方案，可降低开发成本并缩短上市时间。

9.1.1.2 TINA-TI™ 仿真软件（免费下载）

TINA-TI™ 仿真软件是一款简单易用、功能强大且基于 SPICE 引擎的电路仿真程序。TINA-TI 仿真软件是 TINA™ 软件的一款免费全功能版本，除了一系列无源和有源模型外，此版本软件还预先载入了一个宏模型库。TINA-TI 仿真软件提供所有传统的 SPICE 直流、瞬态和频域分析，以及其他设计功能。

TINA-TI 仿真软件提供全面的后处理能力，便于用户以多种方式获得结果，用户可从设计工具和仿真网页免费下载。虚拟仪器提供选择输入波形和探测电路节点、电压以及波形的能力，从而构建一个动态的快速启动工具。

备注

必须安装 TINA 软件或者 TINA-TI 软件后才能使用这些文件。请从 TINA-TI™ 软件文件夹中下载免费的 TINA-TI 仿真软件。

9.1.1.3 滤波器设计工具

滤波器设计工具是一款简单、功能强大且便于使用的有源滤波器设计程序。利用滤波设计器，用户可使用精选 TI 运算放大器和 TI 供应商合作伙伴提供的无源器件来打造理想滤波器设计方案。

设计工具和仿真网页以基于网络的工具形式提供滤波设计工具。用户通过该工具可在短时间内完成多级有源滤波器解决方案的设计、优化和仿真。

9.1.1.4 TI 参考设计

TI 参考设计是由 TI 的精密模拟应用专家创建的模拟解决方案。TI 参考设计提供了许多实用电路的工作原理、组件选择、仿真、完整印刷电路板 (PCB) 电路原理图和布局布线、物料清单以及性能测量结果。TI 参考设计可在线获取，网址为 https://www.ti.com/reference-designs。

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Circuit Board Layout Techniques*
- Texas Instruments, *Op Amps for Everyone* design reference
- Texas Instruments, *OPA140, OPA2140, OPA4140 EMI Immunity Performance* technical brief
- Texas Instruments, *Compensate Transimpedance Amplifiers Intuitively* application report
- Texas Instruments, *Operational amplifier gain stability, Part 3: AC gain-error analysis*
- Texas Instruments, *Operational amplifier gain stability, Part 2: DC gain-error analysis*
- Texas Instruments, *Using infinite-gain, MFB filter topology in fully differential active filters*
- Texas Instruments, *Op Amp Performance Analysis* application bulletin
- Texas Instruments, *Single-Supply Operation of Operational Amplifiers* application bulletin
- Texas Instruments, *Tuning in Amplifiers* application bulletin
- Texas Instruments, *Shelf-Life Evaluation of Lead-Free Component Finishes* application report
- Texas Instruments, *Feedback Plots Define Op Amp AC Performance* application bulletin
- Texas Instruments, *EMI Rejection Ratio of Operational Amplifiers Application Report* application report

9.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*订阅更新*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.4 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

9.5 Trademarks

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WEBENCH® is a registered trademark of Texas Instruments.
PSpice® is a registered trademark of Cadence Design Systems, Inc.
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9.6 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.7 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA140AID	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA140
OPA140AID.B	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA140
OPA140AIDBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O140
OPA140AIDBVR.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O140
OPA140AIDBVRG4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O140
OPA140AIDBVRG4.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O140
OPA140AIDBVT	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O140
OPA140AIDBVT.B	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O140
OPA140AIDGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	Call TI | Nipdau | Nipdau	Level-2-260C-1 YEAR	-40 to 125	(140, O140)
OPA140AIDGKR.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	(140, O140)
OPA140AIDGKRG4	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	140
OPA140AIDGKRG4.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	140
OPA140AIDGKT	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	Call TI | Nipdau | Nipdau	Level-2-260C-1 YEAR	-40 to 125	140
OPA140AIDGKT.B	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	140
OPA140AIDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA140
OPA140AIDR.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA140
OPA140AIDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA140
OPA140AIDRG4.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA140
OPA2140AID	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O2140A
OPA2140AID.B	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O2140A
OPA2140AIDGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	Call TI | Nipdau | Nipdau	Level-2-260C-1 YEAR	-40 to 125	2140
OPA2140AIDGKR.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2140
OPA2140AIDGKT	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	Call TI | Nipdau | Nipdau	Level-2-260C-1 YEAR	-40 to 125	2140
OPA2140AIDGKT.B	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2140
OPA2140AIDGKTG4	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	Call TI | Nipdau	Level-2-260C-1 YEAR	-40 to 125	2140
OPA2140AIDGKTG4.B	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	2140

PACKAGE OPTION ADDENDUM

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA2140AIDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O2140A
OPA2140AIDR.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O2140A
OPA2140AIDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O2140A
OPA2140AIDRG4.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O2140A
OPA2140AIDRGR	Active	Production	SON (DRG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O2140
OPA2140AIDRGR.B	Active	Production	SON (DRG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O2140
OPA2140AIDRGT	Active	Production	SON (DRG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O2140
OPA2140AIDRGT.B	Active	Production	SON (DRG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O2140
OPA4140AID	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	O4140A
OPA4140AID.B	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	O4140A
OPA4140AIDG4	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	O4140A
OPA4140AIDG4.B	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	O4140A
OPA4140AIDR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	O4140A
OPA4140AIDR.B	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	O4140A
OPA4140AIPW	Active	Production	TSSOP (PW) | 14	90 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O4140A
OPA4140AIPW.B	Active	Production	TSSOP (PW) | 14	90 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O4140A
OPA4140AIPWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O4140A
OPA4140AIPWR.B	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O4140A
OPA4140AIPWRG4	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O4140A
OPA4140AIPWRG4.B	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O4140A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

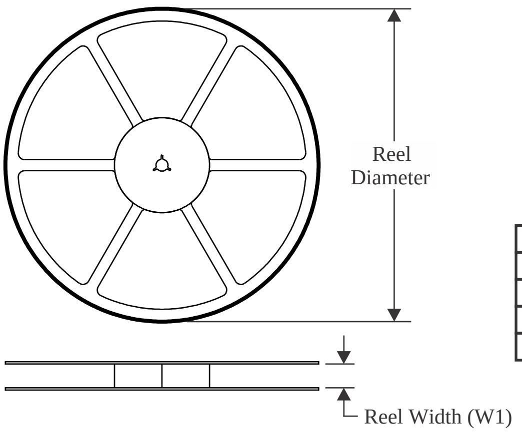
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

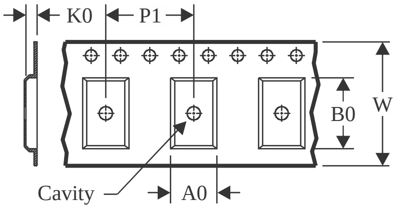
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

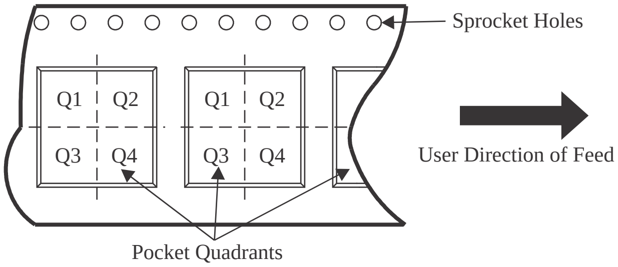


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

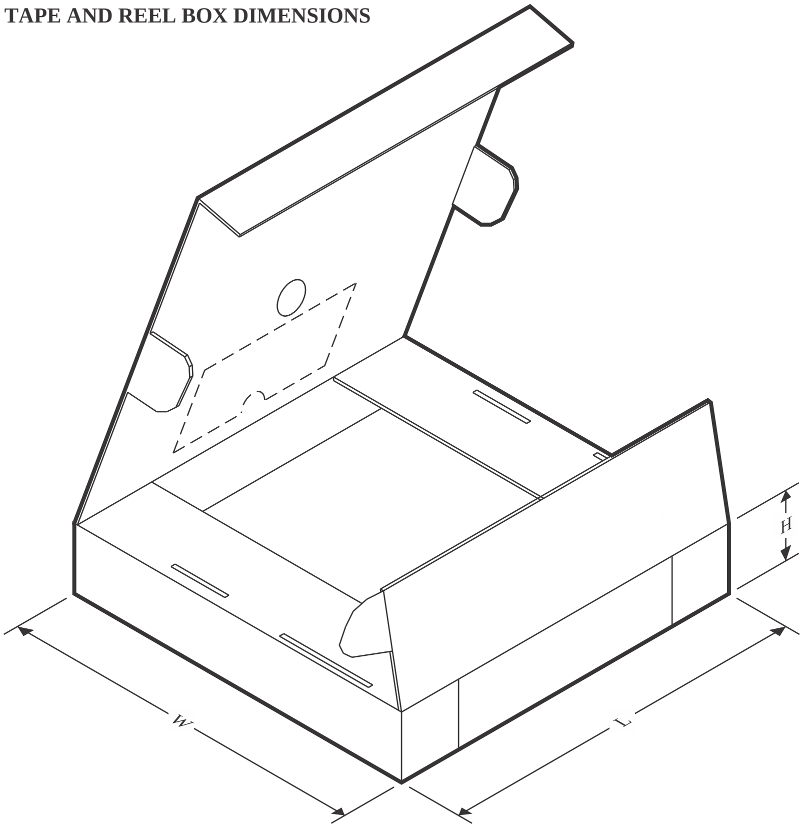


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA140AIDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
OPA140AIDBVRG4	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
OPA140AIDBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
OPA140AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA140AIDGKRG4	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA140AIDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA140AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA140AIDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2140AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2140AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2140AIDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2140AIDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2140AIDGKTG4	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2140AIDGKTG4	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2140AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2140AIDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2140AIDRGR	SON	DRG	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
OPA2140AIDRGT	SON	DRG	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
OPA4140AIDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
OPA4140AIPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
OPA4140AIPWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

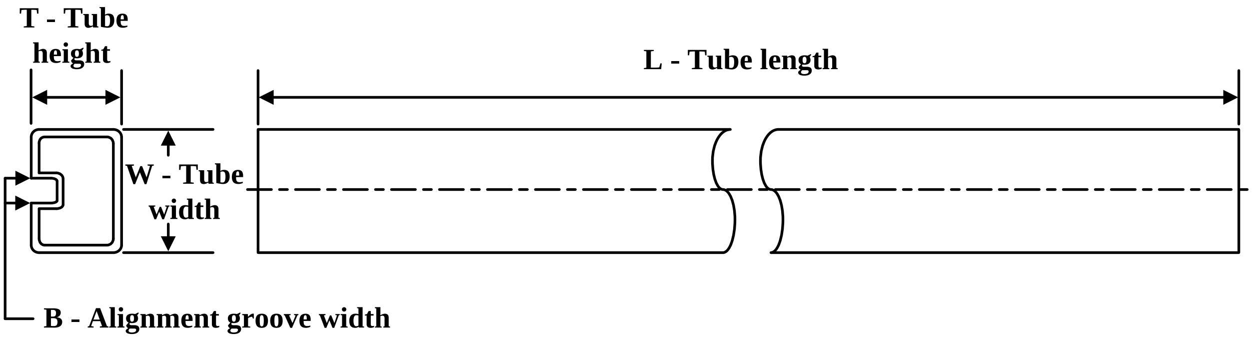


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA140AIDBVR	SOT-23	DBV	5	3000	190.0	190.0	30.0
OPA140AIDBVRG4	SOT-23	DBV	5	3000	190.0	190.0	30.0
OPA140AIDBVT	SOT-23	DBV	5	250	202.0	201.0	28.0
OPA140AIDGKR	VSSOP	DGK	8	2500	356.0	356.0	35.0
OPA140AIDGKRG4	VSSOP	DGK	8	2500	356.0	356.0	35.0
OPA140AIDGKT	VSSOP	DGK	8	250	213.0	191.0	35.0
OPA140AIDR	SOIC	D	8	2500	356.0	356.0	35.0
OPA140AIDRG4	SOIC	D	8	2500	356.0	356.0	35.0
OPA2140AIDGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
OPA2140AIDGKR	VSSOP	DGK	8	2500	356.0	356.0	35.0
OPA2140AIDGKT	VSSOP	DGK	8	250	213.0	191.0	35.0
OPA2140AIDGKT	VSSOP	DGK	8	250	353.0	353.0	32.0
OPA2140AIDGKTG4	VSSOP	DGK	8	250	353.0	353.0	32.0
OPA2140AIDGKTG4	VSSOP	DGK	8	250	213.0	191.0	35.0
OPA2140AIDR	SOIC	D	8	2500	356.0	356.0	35.0
OPA2140AIDRG4	SOIC	D	8	2500	356.0	356.0	35.0
OPA2140AIDRGR	SON	DRG	8	3000	367.0	367.0	35.0
OPA2140AIDRGT	SON	DRG	8	250	210.0	185.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA4140AIDR	SOIC	D	14	2500	356.0	356.0	35.0
OPA4140AIPWR	TSSOP	PW	14	2000	356.0	356.0	35.0
OPA4140AIPWRG4	TSSOP	PW	14	2000	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA140AID	D	SOIC	8	75	506.6	8	3940	4.32
OPA140AID.B	D	SOIC	8	75	506.6	8	3940	4.32
OPA2140AID	D	SOIC	8	75	506.6	8	3940	4.32
OPA2140AID.B	D	SOIC	8	75	506.6	8	3940	4.32
OPA4140AID	D	SOIC	14	50	506.6	8	3940	4.32
OPA4140AID.B	D	SOIC	14	50	506.6	8	3940	4.32
OPA4140AIDG4	D	SOIC	14	50	506.6	8	3940	4.32
OPA4140AIDG4.B	D	SOIC	14	50	506.6	8	3940	4.32
OPA4140AIPW	PW	TSSOP	14	90	508	8.5	3250	2.8
OPA4140AIPW.B	PW	TSSOP	14	90	508	8.5	3250	2.8

GENERIC PACKAGE VIEW

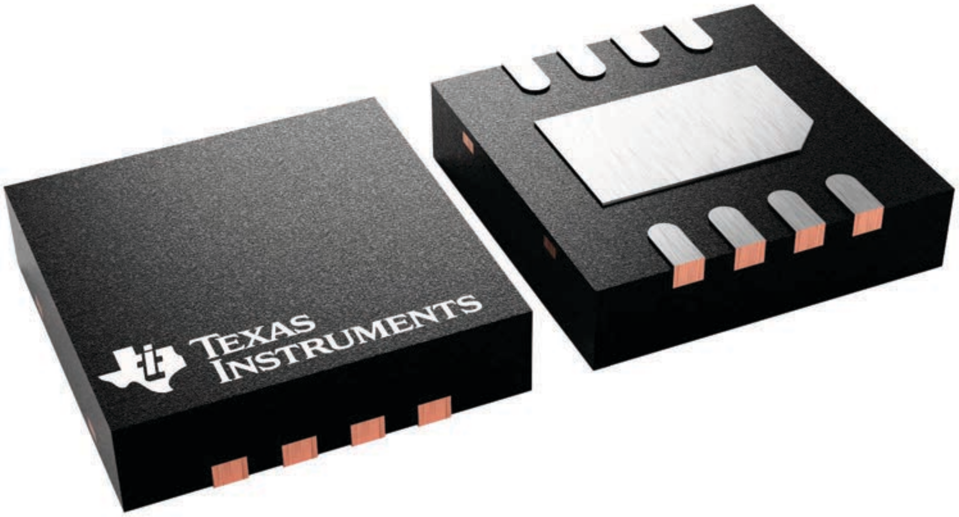
DRG 8

WSON - 0.8 mm max height

3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

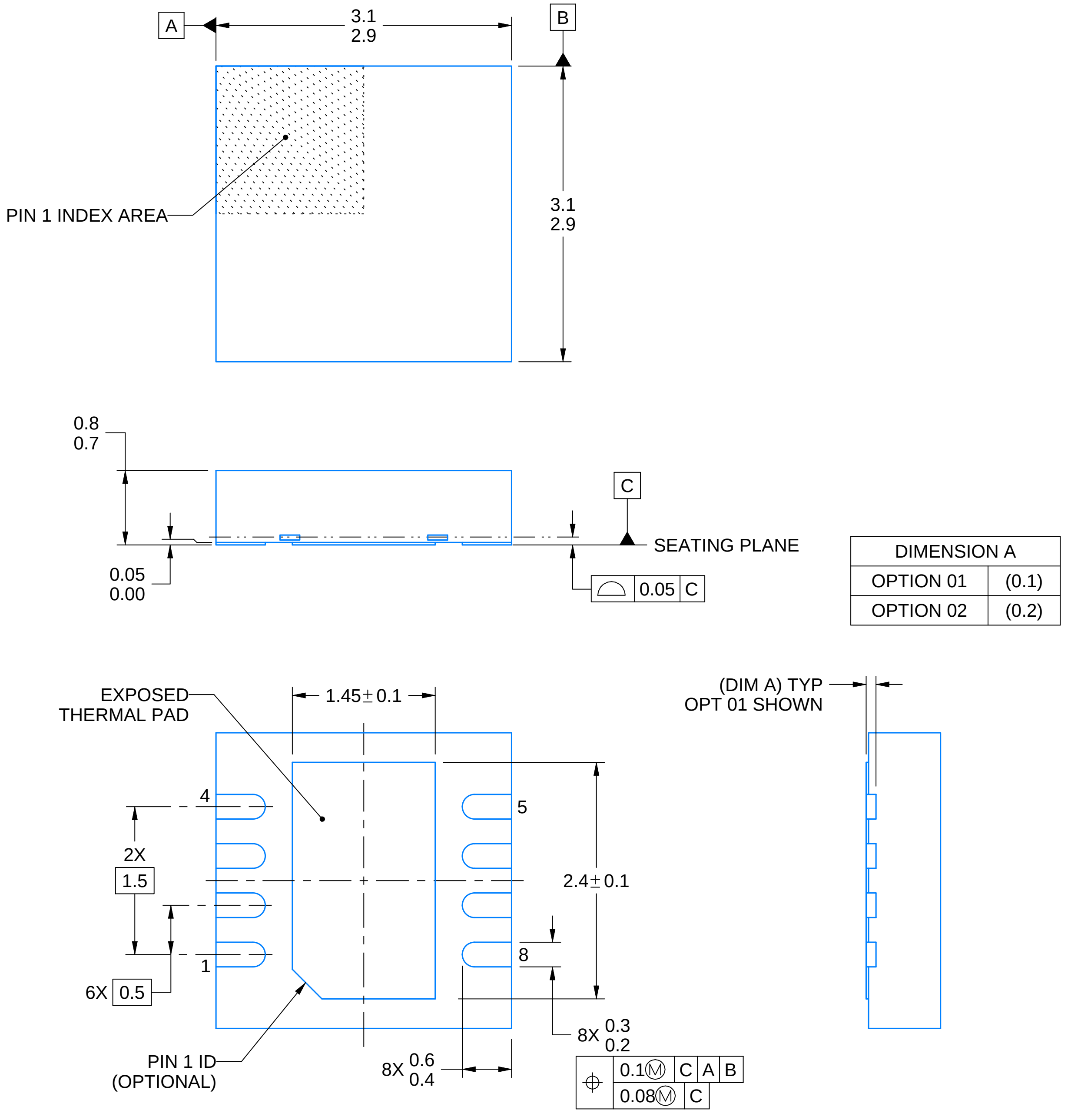


PACKAGE OUTLINE

DRG0008B

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

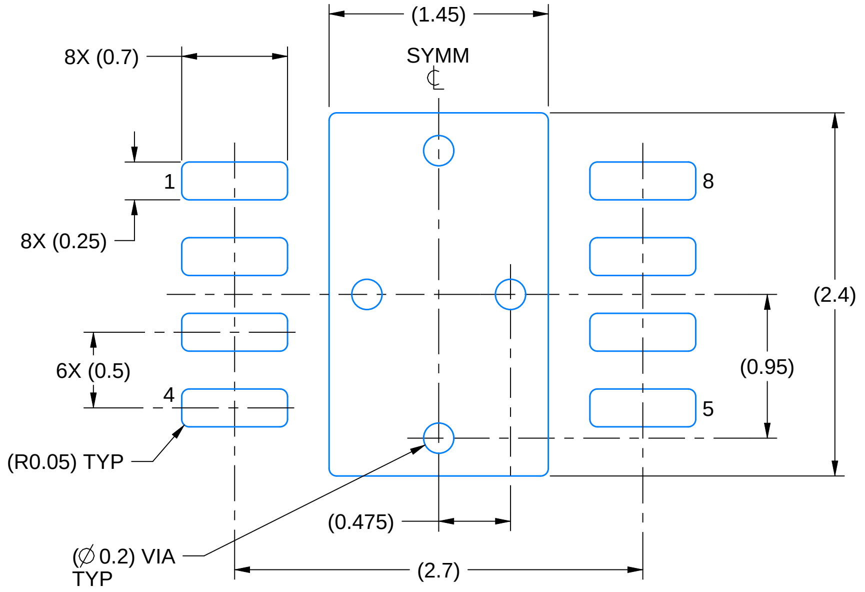


DIMENSION A	
OPTION 01	(0.1)
OPTION 02	(0.2)

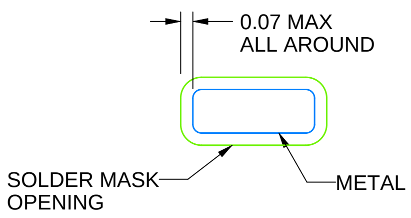
4218886/A 01/2020

NOTES:

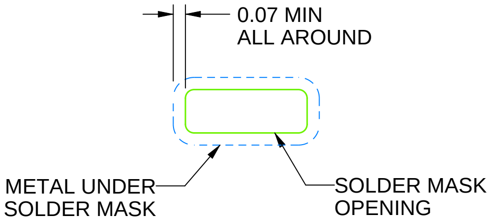
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X



NON SOLDER MASK
DEFINED
(PREFERRED)

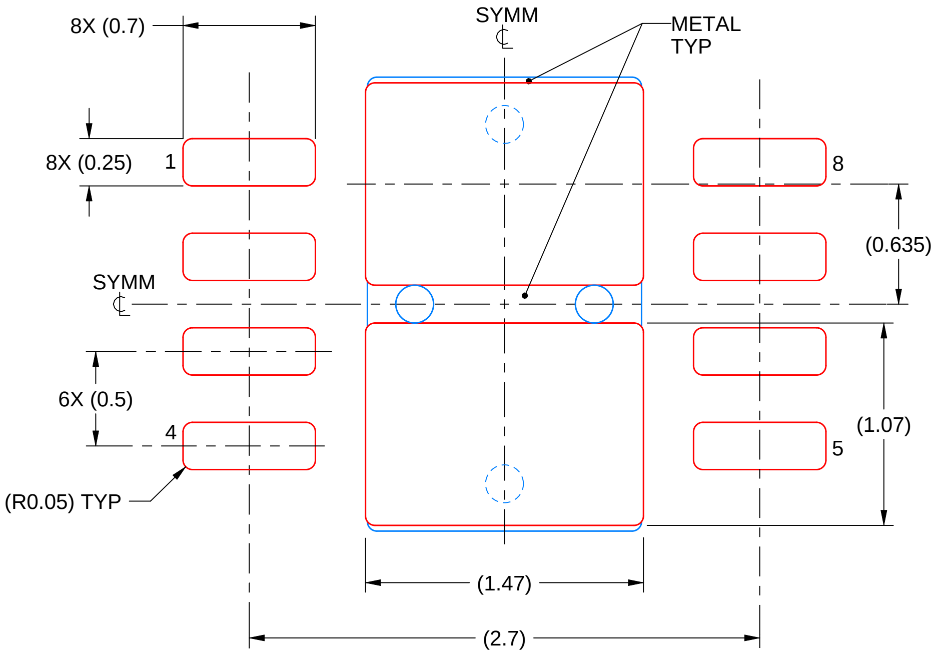


SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



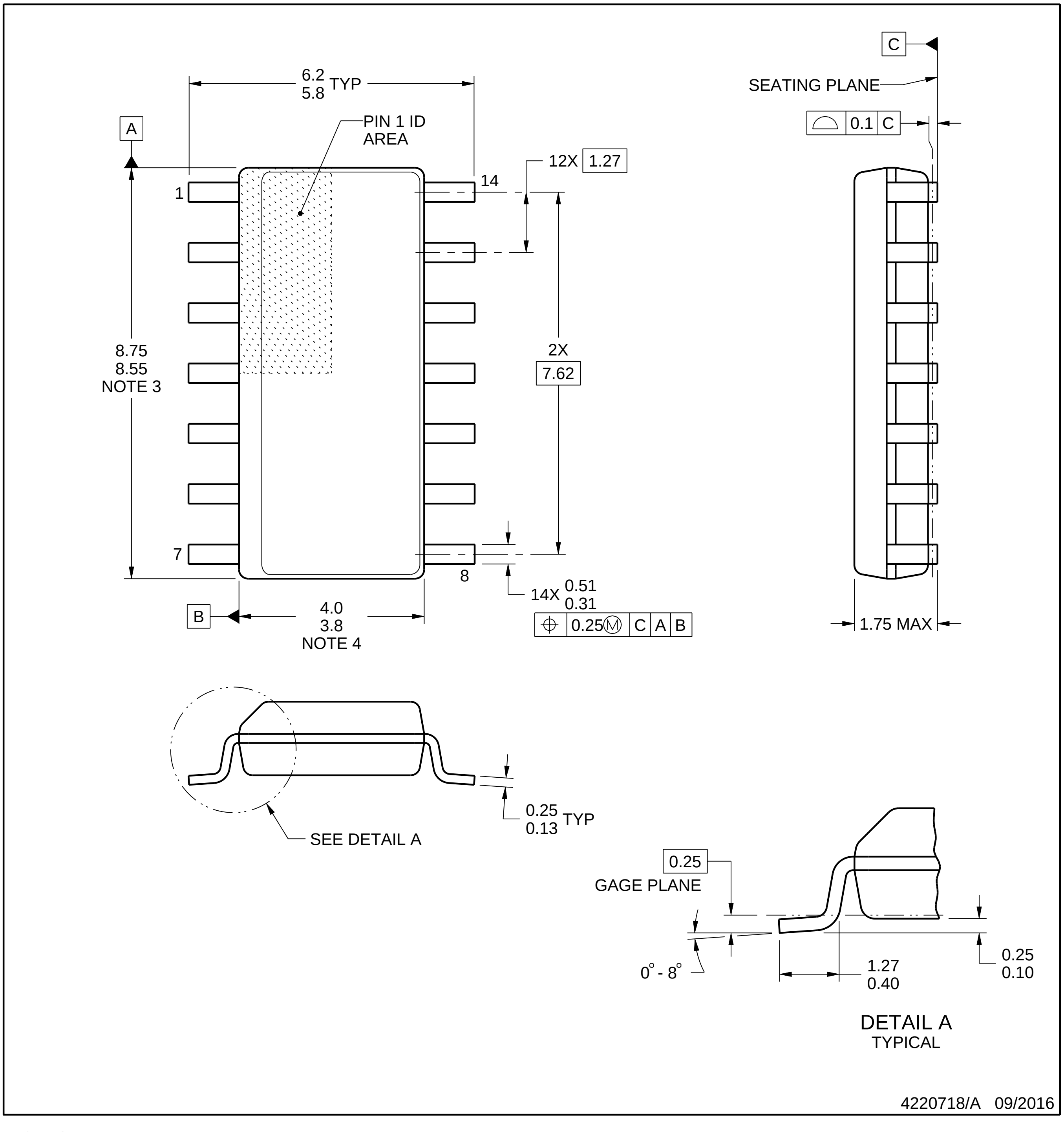
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
82% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218886/A 01/2020

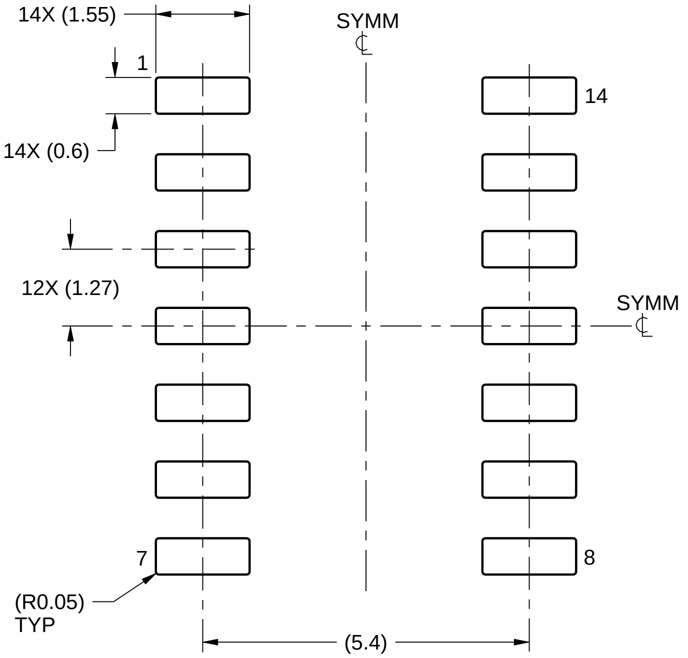
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

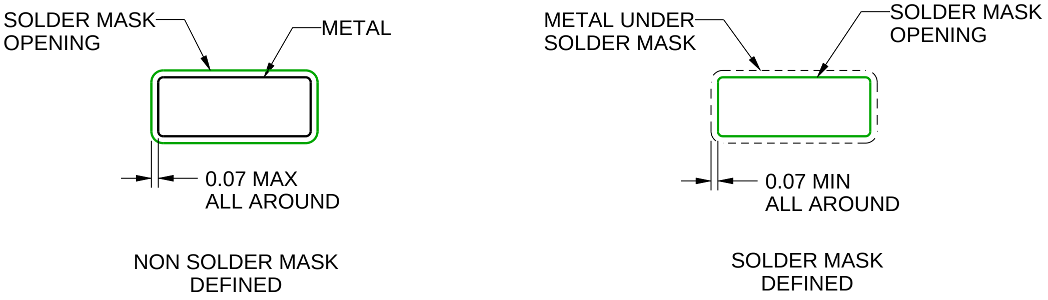


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X

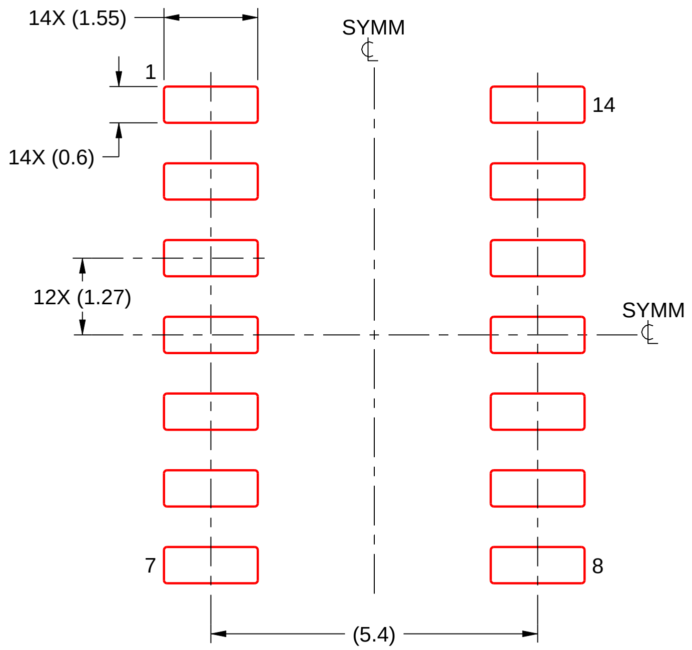


SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

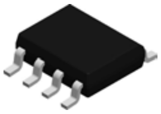


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

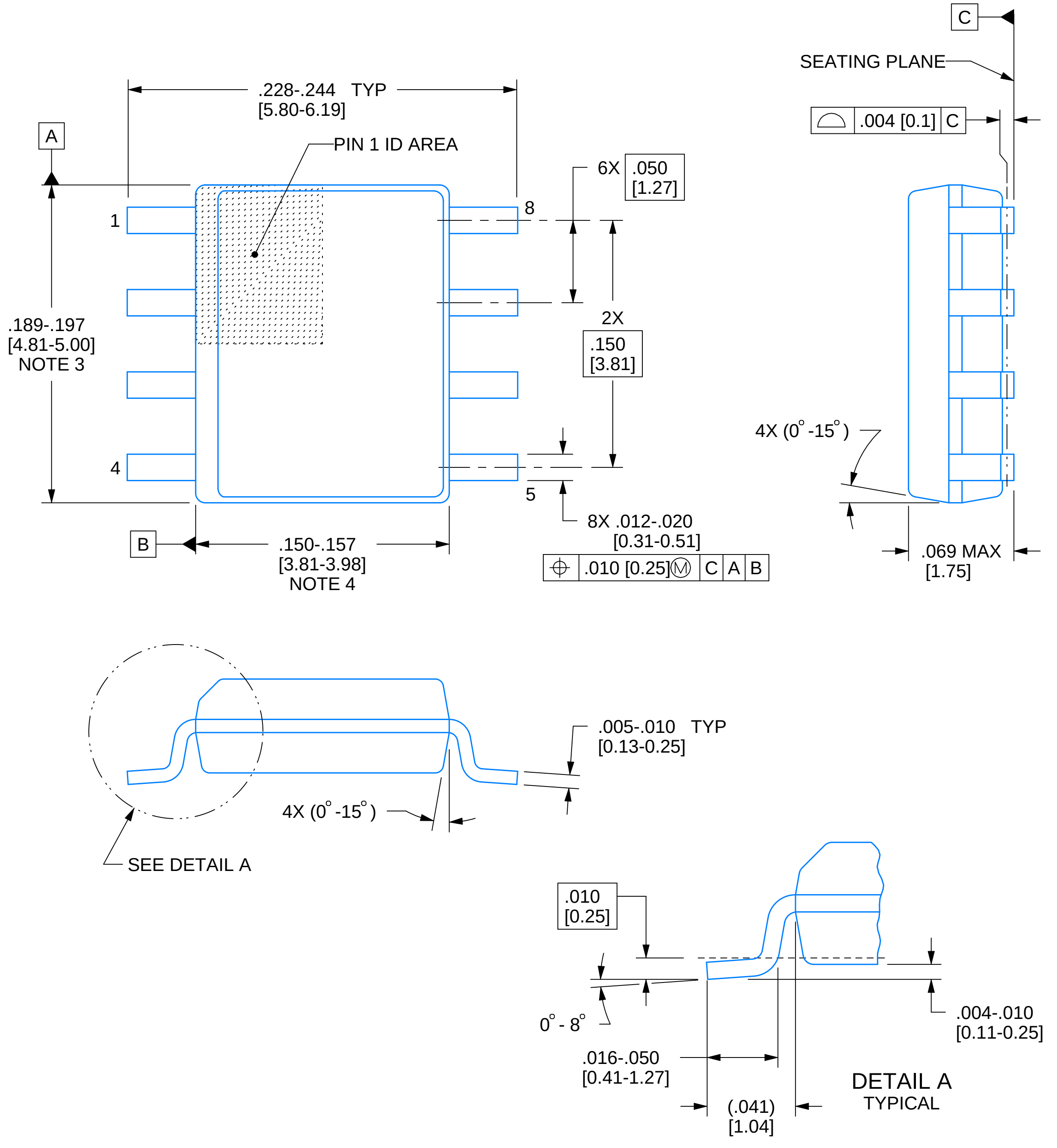


PACKAGE OUTLINE

D0008A

SOIC - 1.75 mm max height

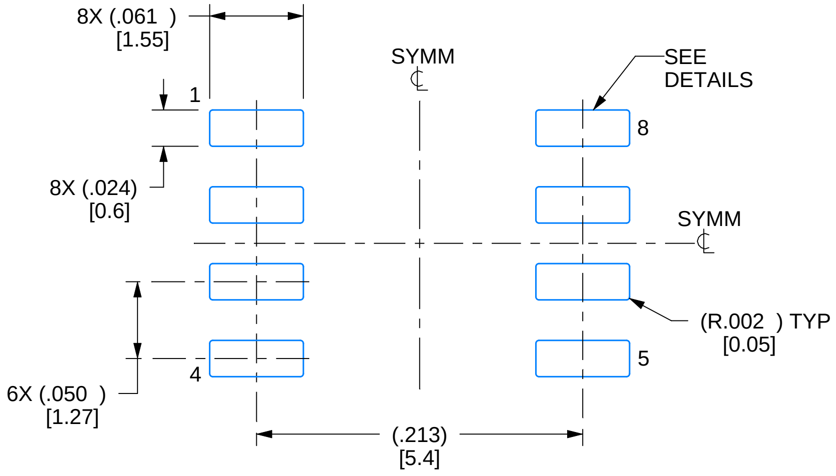
SMALL OUTLINE INTEGRATED CIRCUIT



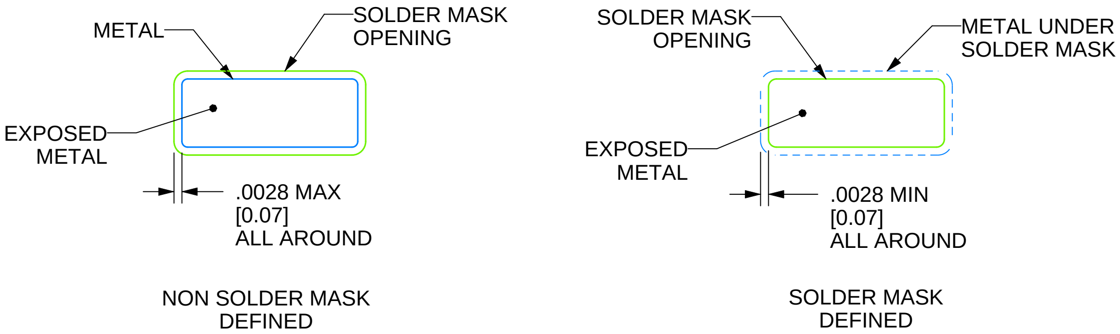
4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



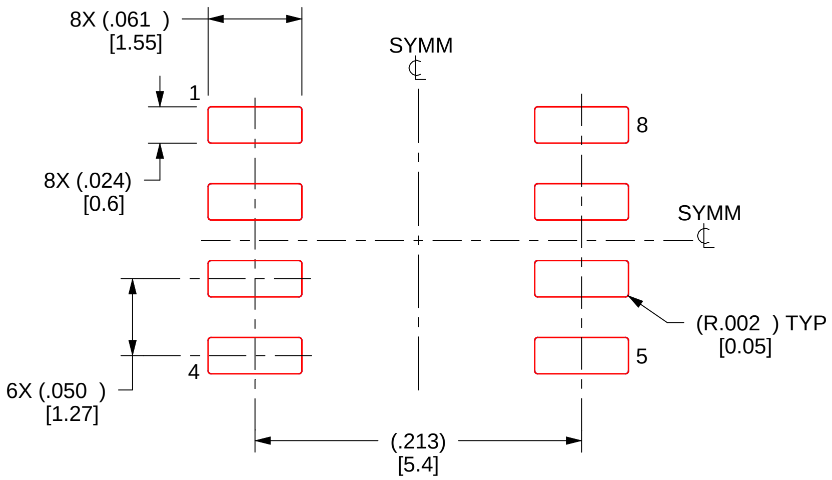
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

NOTES: (continued)

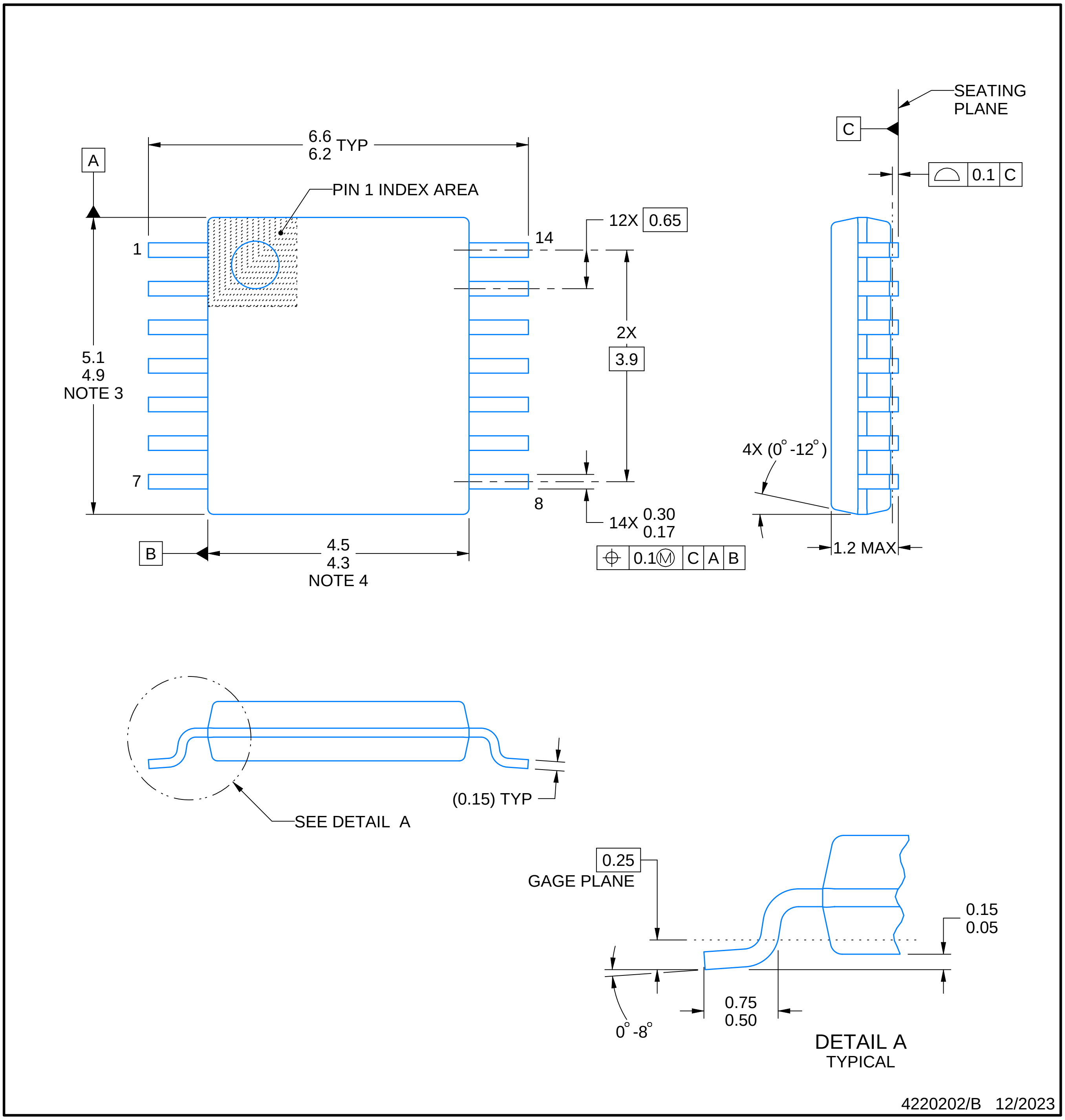
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

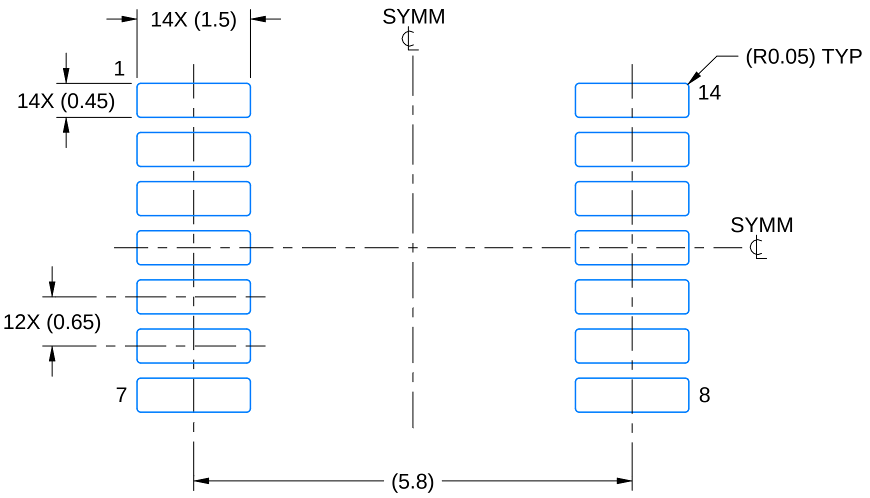
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

NON-SOLDER MASK
DEFINED
(PREFERRED)

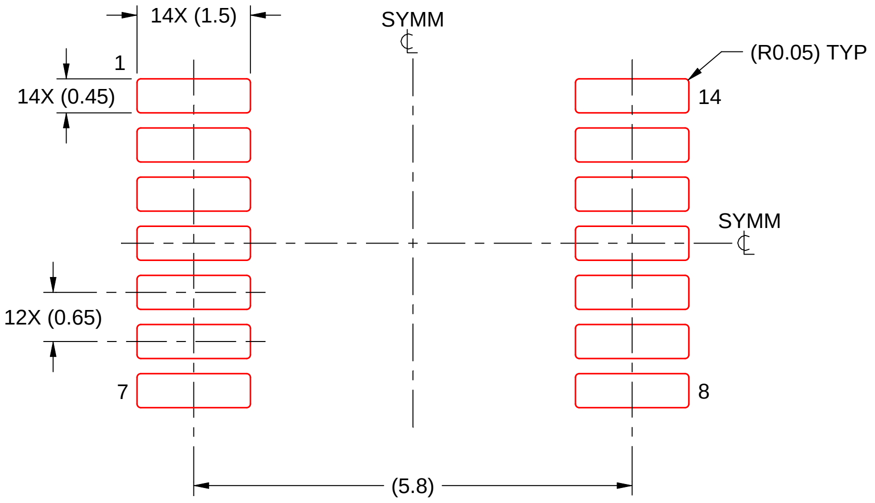
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

NOTES: (continued)

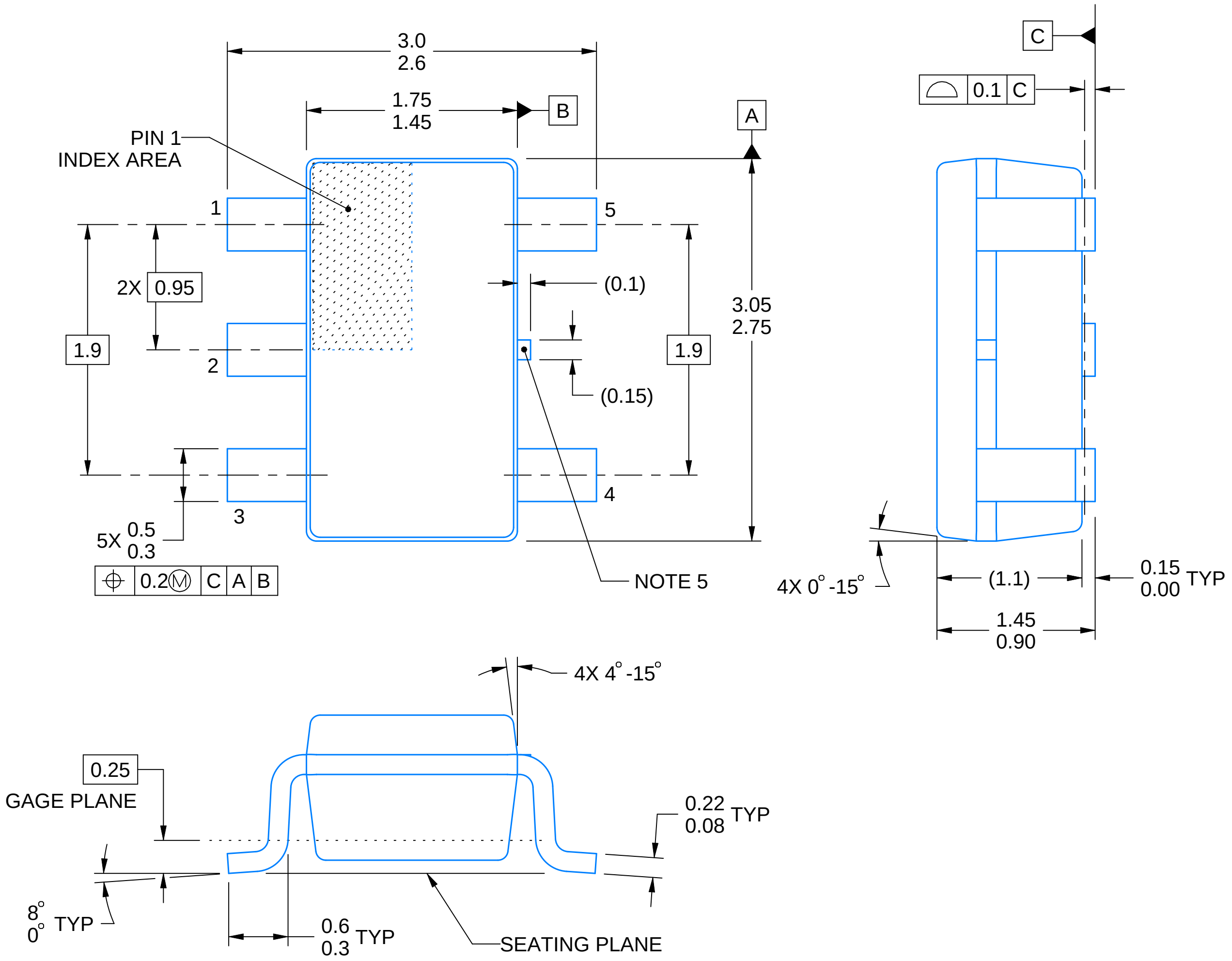
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

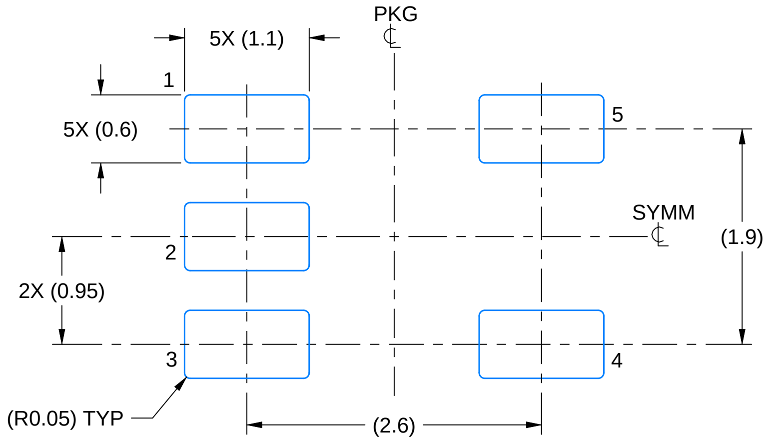
SMALL OUTLINE TRANSISTOR



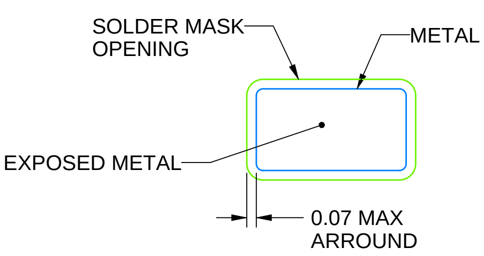
4214839/K 08/2024

NOTES:

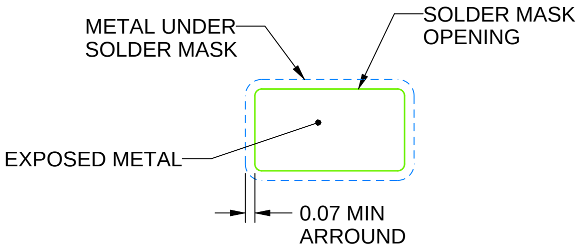
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



NON SOLDER MASK
DEFINED
(PREFERRED)

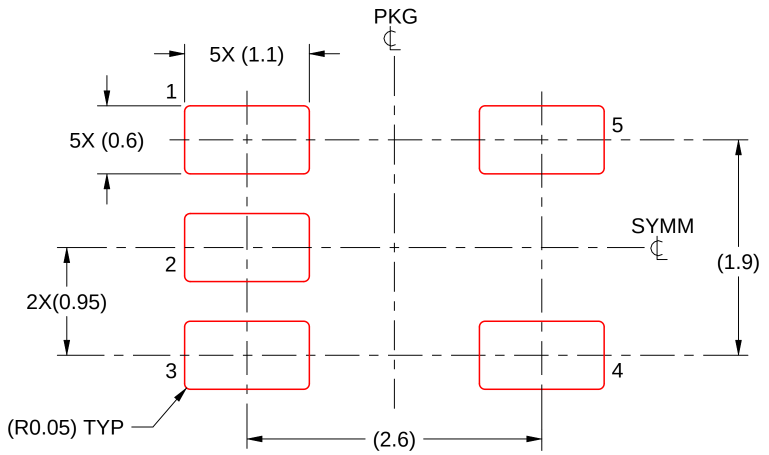


SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

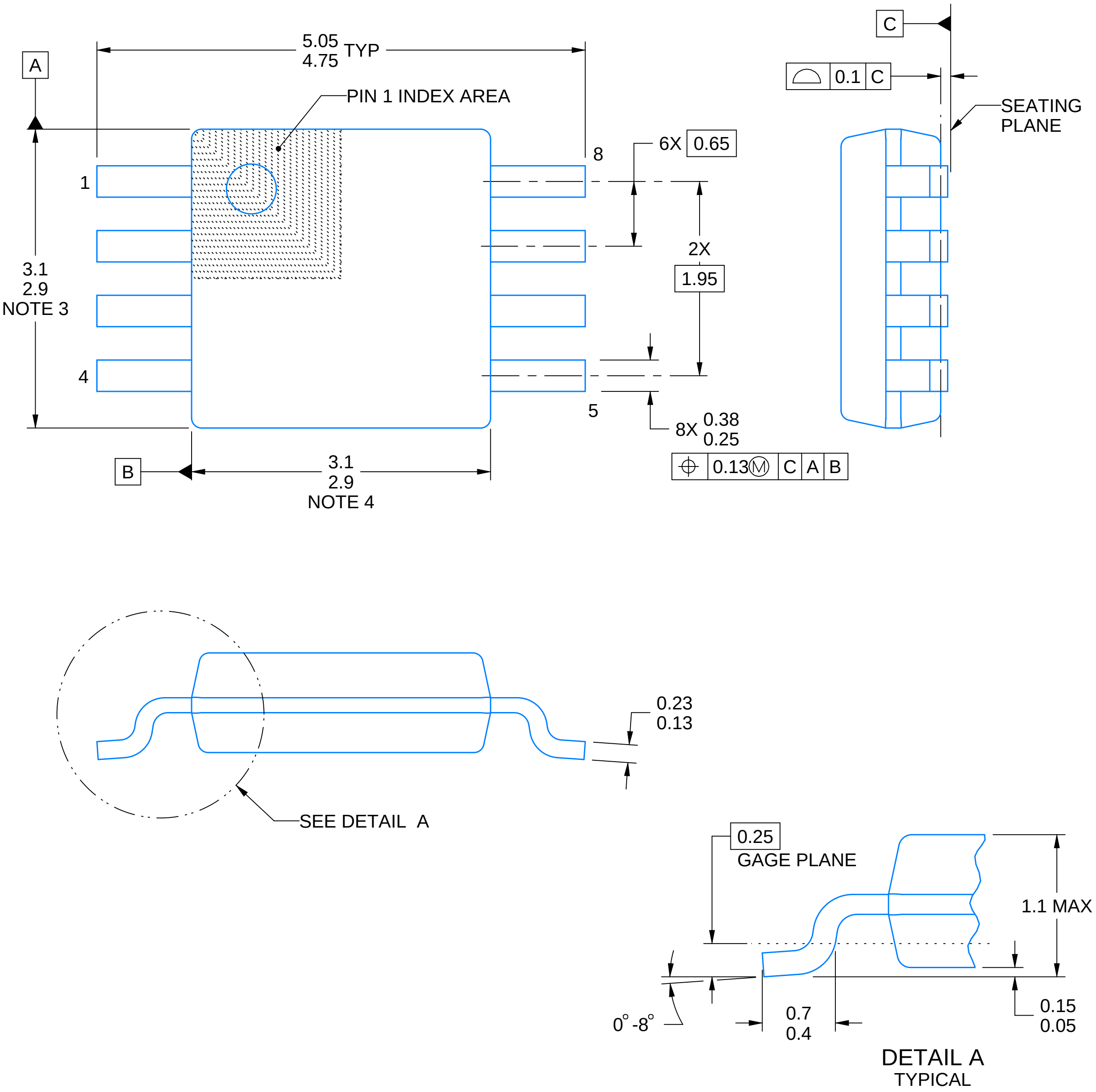


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

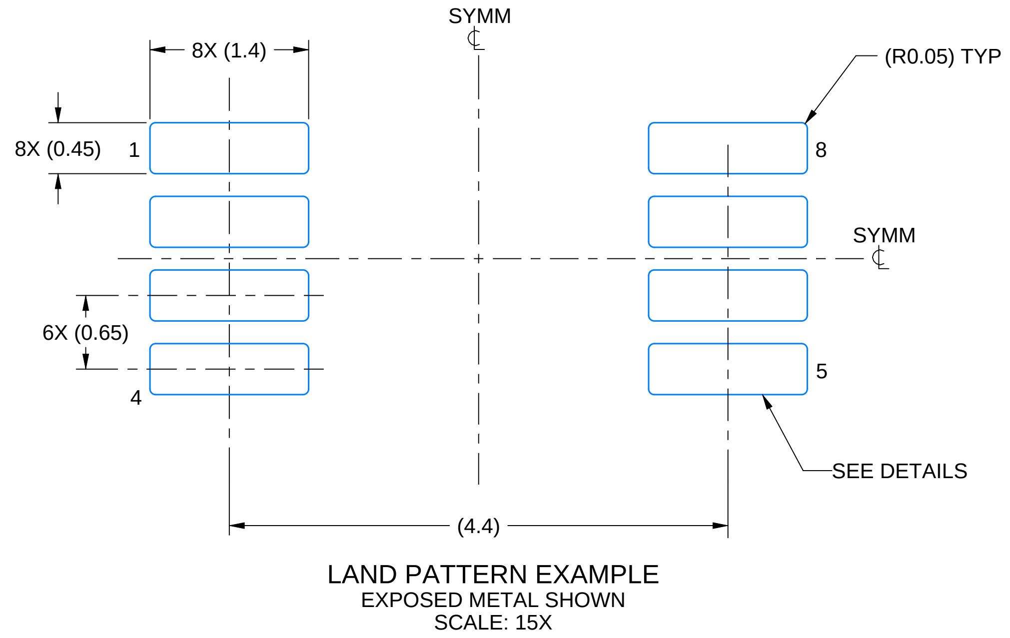


DETAIL A
TYPICAL

PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

NON-SOLDER MASK
DEFINED
(PREFERRED)

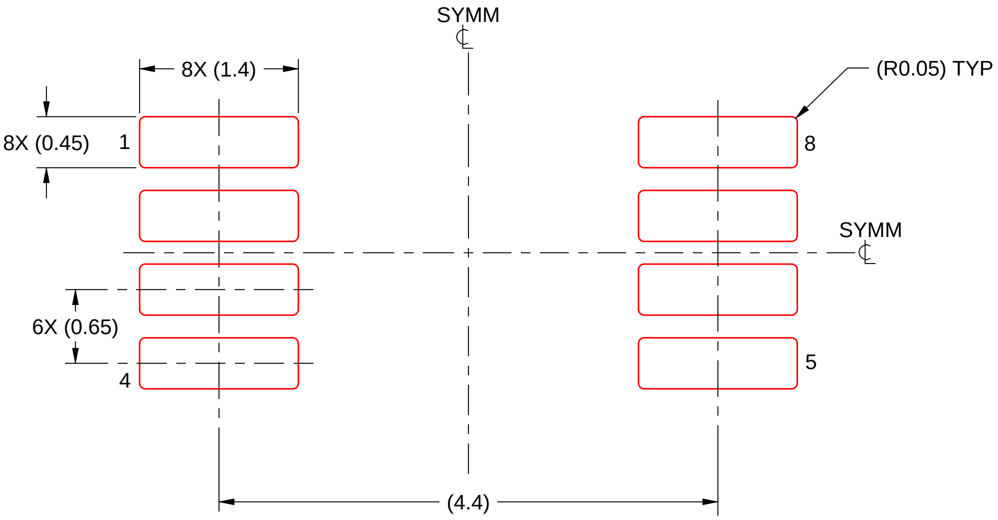
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265